

### Features

- 'HC161, 'HCT161 4-Bit Binary Counter, Asynchronous Reset
- 'HC163, 'HCT163 4-Bit Binary Counter, Synchronous Reset
- Synchronous Counting and Loading
- Two Count Enable Inputs for n-Bit Cascading
- Look-Ahead Carry for High-Speed Counting
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

### Description

The 'HC161, 'HCT161, 'HC163, and 'HCT163 are presettable synchronous counters that feature look-ahead carry logic for use in high-speed counting applications. The 'HC161 and 'HCT161 are asynchronous reset decade and binary counters, respectively; the 'HC163 and 'HCT163 devices are decade and binary counters, respectively, that are reset synchronously with the clock. Counting and parallel presetting are both accomplished synchronously with the negative-to-positive transition of the clock.

A low level on the synchronous parallel enable input, SPE, disables counting operation and allows data at the P0 to P3 inputs to be loaded into the counter (provided that the setup and hold requirements for SPE are met).

All counters are reset with a low level on the Master Reset input, MR. In the 'HC163 and 'HCT163 counters (synchronous reset types), the requirements for setup and hold time with respect to the clock must be met.

Two count enables, PE and TE, in each counter are provided for n-bit cascading. In all counters reset action occurs regardless of the level of the  $\overline{SPE}$ , PE and TE inputs (and the clock input, CP, in the 'HC161 and 'HCT161 types).

If a decade counter is preset to an illegal state or assumes an illegal state when power is applied, it will return to the normal sequence in one count as shown in state diagram.

The look-ahead carry feature simplifies serial cascading of the counters. Both count enable inputs (PE and TE) must be high to count. The TE input is gated with the Q outputs of all four stages so that at the maximum count the terminal count (TC) output goes high for one clock period. This TC pulse is used to enable the next cascaded stage.

### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC161F3A	-55 to 125	16 Ld CERDIP
CD54HC163F3A	-55 to 125	16 Ld CERDIP
CD54HCT163F3A	-55 to 125	16 Ld CERDIP
CD74HC161E	-55 to 125	16 Ld PDIP
CD74HC161M	-55 to 125	16 Ld SOIC
CD74HC161MT	-55 to 125	16 Ld SOIC
CD74HC161M96	-55 to 125	16 Ld SOIC
CD74HC163E	-55 to 125	16 Ld PDIP
CD74HC163M	-55 to 125	16 Ld SOIC
CD74HC163MT	-55 to 125	16 Ld SOIC
CD74HC163M96	-55 to 125	16 Ld SOIC
CD74HCT161E	-55 to 125	16 Ld PDIP
CD74HCT161M	-55 to 125	16 Ld SOIC
CD74HCT161MT	-55 to 125	16 Ld SOIC
CD74HCT161M96	-55 to 125	16 Ld SOIC
CD74HCT163E	-55 to 125	16 Ld PDIP
CD74HCT163M	-55 to 125	16 Ld SOIC
CD74HCT163MT	-55 to 125	16 Ld SOIC
CD74HCT163M96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

# CD54/74HC161, CD54/74HCT161, CD54/74HC163, CD54/74HCT163

## Pinout

CD54HC161, CD54HCT161, CD54HC163, CD54HCT163  
(CERDIP)  
CD74HC161, CD74HCT161, CD74HC163, CD74HCT163  
(PDIP, SOIC)  
TOP VIEW



## Functional Diagram



**CD54/74HC161, CD54/74HCT161, CD54/74HC163, CD54/74HCT163**

**MODE SELECT - FUNCTION TABLE FOR 'HC161 AND 'HCT161**

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	PE	TE	$\overline{SP\overline{E}}$	$P_n$	$Q_n$	TC
Reset (Clear)	L	X	X	X	X	X	L	L
Parallel Load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	(Note 1)
Count	H	↑	h	h	h (Note 3)	X	Count	(Note 1)
Inhibit	H	X	l (Note 2)	X	h (Note 3)	X	$q_n$	(Note 1)
	H	X	X	l (Note 2)	h (Note 3)	X	$q_n$	L

**MODE SELECT - FUNCTION TABLE FOR 'HC163 AND 'HCT163**

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	PE	TE	$\overline{SP\overline{E}}$	$P_n$	$Q_n$	TC
Reset (Clear)	l	↑	X	X	X	X	L	L
Parallel Load	h (Note 3)	↑	X	X	l	l	L	L
	h (Note 3)	↑	X	X	l	h	H	(Note 1)
Count	h (Note 3)	↑	h	h	h (Note 3)	X	Count	(Note 1)
Inhibit	h (Note 3)	X	l (Note 2)	X	h (Note 3)	X	$q_n$	(Note 1)
	h (Note 3)	X	X	l (Note 2)	h (Note 3)	X	$q_n$	L

H = High voltage level steady state; L = Low voltage level steady state; h = High voltage level one setup time prior to the Low-to-High clock transition; l = Low voltage level one setup time prior to the Low-to-High clock transition; X = Don't Care; q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition; ↑ = Low-to-High clock transition.

**NOTES:**

1. The TC output is High when TE is High and the counter is at Terminal Count (HHHH for HC/HCT161 and 'HC/HCT163).
2. The High-to-Low transition of PE or TE on the 'HC/HCT161 and the 'HC/HCT163 should only occur while CP is HIGH for conventional operation.
3. The Low-to-High transition of  $\overline{SP\overline{E}}$  on the 'HC/HCT161 and  $\overline{SP\overline{E}}$  or  $\overline{MR}$  on the 'HC/HCT163 should only occur while CP is HIGH for conventional operation.

# CD54/74HC161, CD54/74HCT161, CD54/74HC163, CD54/74HCT163

## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 7V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Drain Current, per Output, $I_O$	
For $-0.5V < V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ .....	$\pm 50mA$

## Thermal Information

Thermal Resistance (Typical, Note 4)	$\theta_{JA}$ ( $^{\circ}C/W$ )
E (PDIP) Package .....	67
M (SOIC) Package .....	73
Maximum Junction Temperature .....	150 $^{\circ}C$
Maximum Storage Temperature Range .....	-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s) .....	300 $^{\circ}C$ (SOIC - Lead Tips Only)

## Operating Conditions

Temperature Range, $T_A$ .....	-55 $^{\circ}C$ to 125 $^{\circ}C$
Supply Voltage Range, $V_{CC}$	
HC Types .....	.2V to 6V
HCT Types .....	4.5V to 5.5V
DC Input or Output Voltage, $V_I, V_O$ .....	0V to $V_{CC}$
Input Rise and Fall Time	
2V .....	1000ns (Max)
4.5V .....	500ns (Max)
6V .....	400ns (Max)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

### NOTE:

- The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25 $^{\circ}C$			-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS	
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX		
<b>HC TYPES</b>													
High Level Input Voltage	$V_{IH}$	-	-	2	1.5	-	-	1.5	-	1.5	-	V	
				4.5	3.15	-	-	3.15	-	3.15	-	V	
				6	4.2	-	-	4.2	-	4.2	-	V	
Low Level Input Voltage	$V_{IL}$	-	-	2	-	-	0.5	-	0.5	-	0.5	V	
				4.5	-	-	1.35	-	1.35	-	1.35	V	
				6	-	-	1.8	-	1.8	-	1.8	V	
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-	-	-	-	-	-	-	-	-	V	
			-4	-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	-	-	-	-	-	-	-	-	-	V	
			4	4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	$I_I$	$V_{CC}$ or GND	-	6	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu A$	

**CD54/74HC161, CD54/74HCT161, CD54/74HC163, CD54/74HCT163**

**DC Electrical Specifications (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	6	-	-	8	-	80	-	160	μA
<b>HCT TYPES</b>												
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> and GND	0	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	-	8	-	80	-	160	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI <sub>CC</sub> (Note 5)	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

5. For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

**HCT Input Loading Table**

INPUT	UNIT LOADS
P0 - P3	0.25
PE	0.65
CP	1.05
MR	0.8
SPE	0.5
TE	1.05

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Table, e.g., 360μA max at 25°C.

**CD54/74HC161, CD54/74HCT161, CD54/74HC163, CD54/74HCT163**

**Prerequisite For Switching Specifications**

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
Maximum CP Frequency (Note 6)	f <sub>MAX</sub>	-	2	6	-	-	5	-	4	-	MHz
			4.5	30	-	-	24	-	20	-	MHz
			6	35	-	-	28	-	24	-	MHz
CP Width (Low)	t <sub>W(L)</sub>	-	2	80	-	-	100	-	120	-	ns
			4.5	16	-	-	20	-	24	-	ns
			6	14	-	-	17	-	20	-	ns
MR Pulse Width (161)	t <sub>W</sub>	-	2	100	-	-	125	-	150	-	ns
			4.5	20	-	-	25	-	30	-	ns
			6	17	-	-	21	-	26	-	ns
Setup Time, Pn to CP	t <sub>SU</sub>	-	2	60	-	-	75	-	90	-	ns
			4.5	12	-	-	15	-	18	-	ns
			6	10	-	-	13	-	15	-	ns
Setup Time, PE or TE to CP	t <sub>SU</sub>	-	2	50	-	-	65	-	75	-	ns
			4.5	10	-	-	13	-	15	-	ns
			6	9	-	-	11	-	13	-	ns
Setup Time, SPE to CP	t <sub>SU</sub>	-	2	60	-	-	75	-	90	-	ns
			4.5	12	-	-	15	-	18	-	ns
			6	10	-	-	13	-	15	-	ns
Setup Time, MR to CP (163)	t <sub>SU</sub>	-	2	65	-	-	80	-	100	-	ns
			4.5	13	-	-	16	-	20	-	ns
			6	11	-	-	14	-	17	-	ns
Hold Time, PN to CP	t <sub>H</sub>	-	2	3	-	-	3	-	3	-	ns
			4.5	3	-	-	3	-	3	-	ns
			6	3	-	-	3	-	3	-	ns
Hold Time, TE or PE to CP	t <sub>H</sub>	-	2	0	-	-	0	-	0	-	ns
			4.5	0	-	-	0	-	0	-	ns
			6	0	-	-	0	-	0	-	ns
Hold Time, SPE to CP	t <sub>H</sub>	-	2	0	-	-	0	-	0	-	ns
			4.5	0	-	-	0	-	0	-	ns
			6	0	-	-	0	-	0	-	ns
Recovery Time, MR to CP (161)	t <sub>REC</sub>	-	2	75	-	-	95	-	110	-	ns
			4.5	15	-	-	19	-	22	-	ns
			6	13	-	-	16	-	19	-	ns

**CD54/74HC161, CD54/74HCT161, CD54/74HC163, CD54/74HCT163**

**Prerequisite For Switching Specifications (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HCT TYPES</b>											
Maximum CP Frequency	f <sub>MAX</sub>	-	4.5	30	-	-	24	-	20	-	MHz
CP Width (Low) (Note 6)	t <sub>W(L)</sub>	-	4.5	16	-	-	20	-	24	-	ns
$\overline{MR}$ Pulse Width (161)	t <sub>W</sub>	-	4.5	20	-	-	25	-	30	-	ns
Setup Time, Pn to CP	t <sub>SU</sub>	-	4.5	10	-	-	13	-	15	-	ns
Setup Time, PE or TE to CP	t <sub>SU</sub>	-	4.5	13	-	-	16	-	20	-	ns
Setup Time, $\overline{SPE}$ to CP	t <sub>SU</sub>	-	4.5	12	-	-	15	-	18	-	ns
Setup Time, $\overline{MR}$ to CP (163)	t <sub>SU</sub>	-	4.5	13	-	-	16	-	20	-	ns
Hold Time, PN to CP	t <sub>H</sub>	-	4.5	5	-	-	5	-	5	-	ns
Hold Time, TE or PE to CP	t <sub>H</sub>	-	4.5	3	-	-	3	-	3	-	ns
Hold Time, $\overline{SPE}$ to CP	t <sub>H</sub>	-	4.5	3	-	-	3	-	3	-	ns
Recovery Time, $\overline{MR}$ to CP (161)	t <sub>REC</sub>	-	4.5	15	-	-	19	-	22	-	ns

NOTE:

6. Applies to non-cascaded operation only. With cascaded counters clock to terminal count propagation delays, count enables (PE or TE)-to-clock setup times, and count enables (PE or TE)-to-clock hold times determine maximum clock frequency. For example with these HC devices:

$$f_{MAX} (CP) = \frac{1}{CP\text{-to-TC prop. delay} + TE\text{-to-CP setup} + TE\text{-to-CP Hold}} = \frac{1}{37 + 10 + 0} \approx 21\text{MHz}(\text{min})$$

**Switching Specifications** C<sub>L</sub> = 50pF, Input t<sub>r</sub>, t<sub>f</sub> = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
Propagation Delay CP to TC	t <sub>PHL</sub> , t <sub>PLH</sub>	C <sub>L</sub> = 50pF	2	-	-	185	-	230	-	280	ns
			4.5	-	-	37	-	46	-	56	ns
		C <sub>L</sub> = 15pF	5	-	15	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	31	-	39	-	48	ns
CP to Qn	t <sub>PHL</sub> , t <sub>PLH</sub>	C <sub>L</sub> = 50pF	2	-	-	185	-	230	-	280	ns
			4.5	-	-	37	-	46	-	56	ns
		C <sub>L</sub> = 15pF	5	-	15	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	31	-	39	-	48	ns
TE to TC	t <sub>PHL</sub> , t <sub>PLH</sub>	C <sub>L</sub> = 50pF	2	-	-	120	-	150	-	180	ns
			4.5	-	-	24	-	30	-	36	ns
		C <sub>L</sub> = 15pF	5	-	9	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	20	-	26	-	31	ns

**CD54/74HC161, CD54/74HCT161, CD54/74HC163, CD54/74HCT163**

**Switching Specifications**  $C_L = 50\text{pF}$ , Input  $t_r$ ,  $t_f = 6\text{ns}$  (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$\overline{MR}$ to Qn (161)	$t_{PHL}$	$C_L = 50\text{pF}$	2	-	-	210	-	265	-	315	ns
			4.5	-	-	42	-	53	-	63	ns
		$C_L = 15\text{pF}$	5	-	18	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	36	-	45	-	54	ns
$\overline{MR}$ to TC (161)	$t_{PHL}$	$C_L = 50\text{pF}$	2	-	-	210	-	265	-	315	ns
			4.5	-	-	42	-	53	-	63	ns
		$C_L = 50\text{pF}$	6	-	-	36	-	45	-	54	ns
Output Transition Time	$t_{THL}, t_{TLH}$	$C_L = 50\text{pF}$	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Power Dissipation Capacitance (Notes 7, 8)	$C_{PD}$	-	5	-	60	-	-	-	-	-	pF
Input Capacitance	$C_{IN}$	$C_L = 50\text{pF}$	-	10	-	10	-	10	-	10	pF

**HCT TYPES**

Propagation Delay CP to TC	$t_{PHL}, t_{PLH}$	$C_L = 50\text{pF}$	4.5	-	-	42	-	53	-	63	ns
		$C_L = 15\text{pF}$	5	-	18	-	-	-	-	-	ns
CP to Qn	$t_{PHL}, t_{PLH}$	$C_L = 50\text{pF}$	4.5	-	-	39	-	49	-	59	ns
		$C_L = 15\text{pF}$	5	-	16	-	-	-	-	-	ns
TE to TC	$t_{PHL}, t_{PLH}$	$C_L = 50\text{pF}$	4.5	-	-	32	-	40	-	48	ns
		$C_L = 15\text{pF}$	5	-	13	-	-	-	-	-	ns
$\overline{MR}$ to Qn (161)	$t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	-	50	-	63	-	75	ns
		$C_L = 15\text{pF}$	5	-	21	-	-	-	-	-	ns
$\overline{MR}$ to TC (161)	$t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	-	50	-	63	-	75	ns
Output Transition Time	$t_{THL}, t_{TLH}$	$C_L = 50\text{pF}$	4.5	-	-	15	-	19	-	22	ns
Power Dissipation Capacitance (Notes 7, 8)	$C_{PD}$	-	5	-	63	-	-	-	-	-	pF
Input Capacitance	$C_{IN}$	$C_L = 50\text{pF}$	-	10	-	10	-	10	-	10	pF

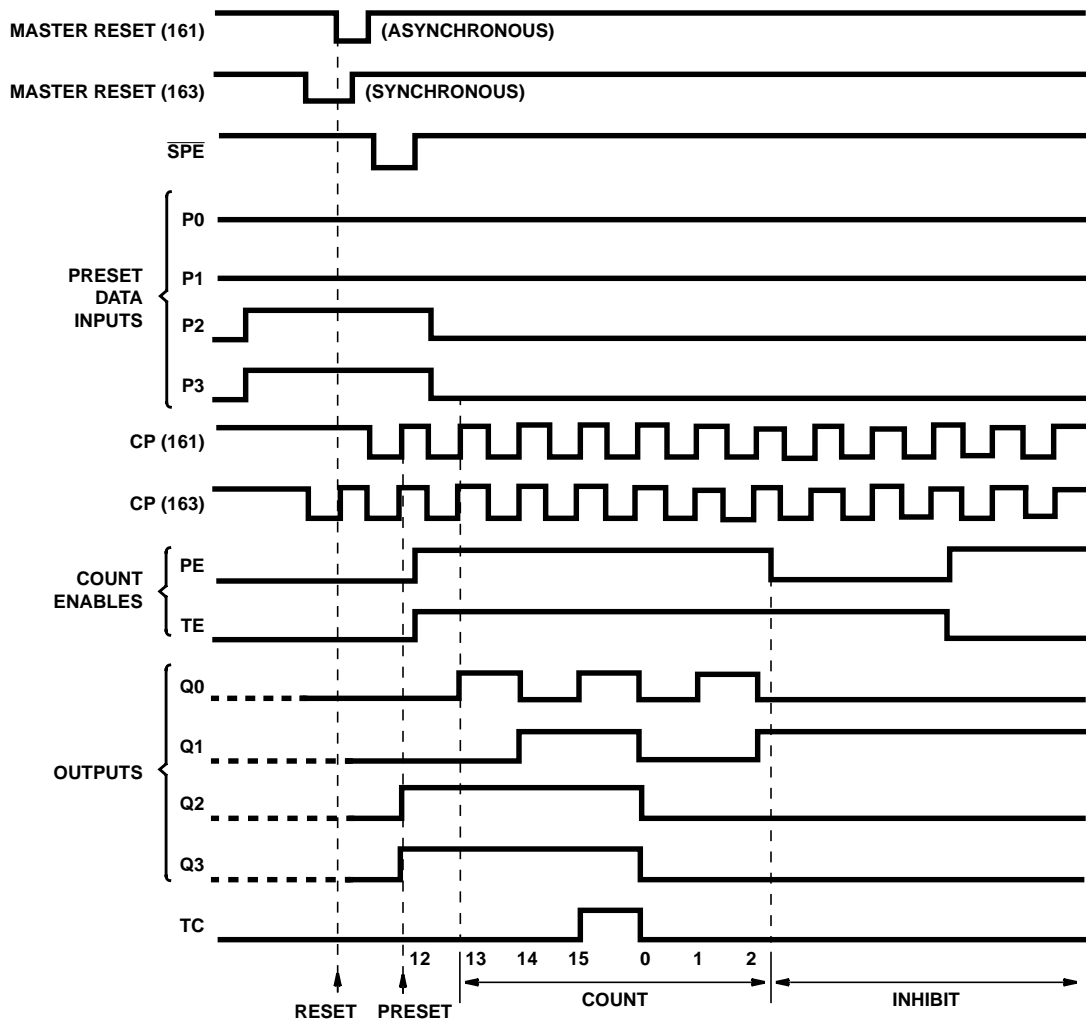
**NOTES:**

7.  $C_{PD}$  is used to determine the dynamic power consumption, per package.

8.  $P_D = C_{PD} V_{CC}^2 f_i + \sum(C_L V_{CC}^2 f_O)$  where  $f_i$  = Input Frequency,  $f_O$  = Output Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.



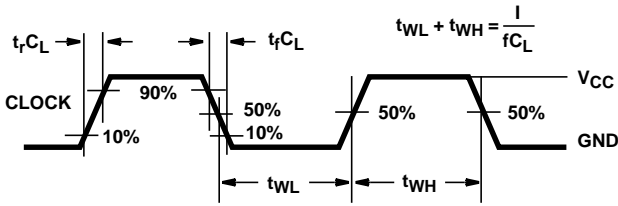
**Timing Diagram**



Sequence illustrated on waveforms:

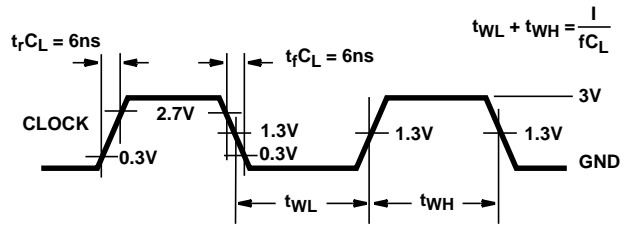
1. Reset outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit.

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

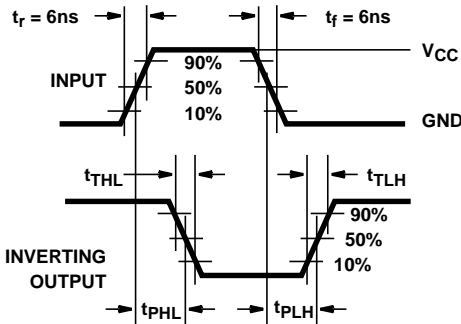


FIGURE 3. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

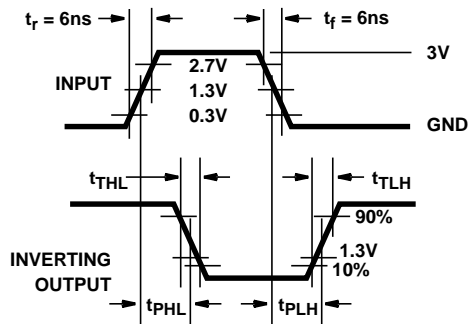


FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC



FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

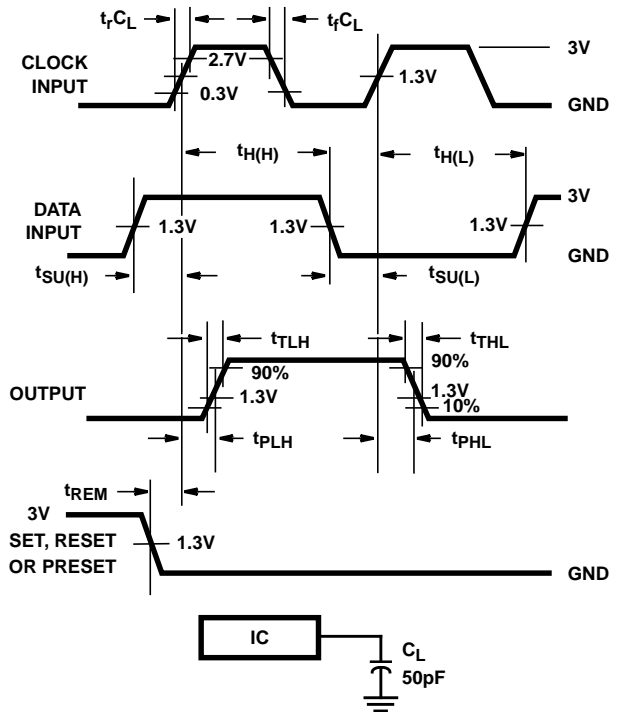


FIGURE 6. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CD54HC161F	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
CD54HC161F3A	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
CD54HC163F3A	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
CD54HCT161F3A	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
CD54HCT163F	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
CD54HCT163F3A	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
CD74HC161E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HC161M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC161M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC161M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC161ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC161MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC161MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC163E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HC163EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HC163M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC163M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC163M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC163ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC163MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC163MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT161E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HCT161M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT161M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT161M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT161ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT161MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CD74HCT161MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT163E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HCT163EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HCT163M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT163M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT163M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT163ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT163MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT163MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AC.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<b>Products</b>		<b>Applications</b>	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
		Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265