

CD4031B Types

CMOS 64-Stage Static Shift Register

High-Voltage Types (20-Volt Rating)

■ CD4031B is a static shift register that contains 64 D-type, master-slave flip-flop stages and one stage which is a D-type master flip-flop only (referred to as a 1/2 stage).

The logic level present at the DATA input is transferred into the first stage and shifted one stage at each positive-going clock transition. Maximum clock frequencies up to 12 Megahertz (typical) can be obtained. Because fully static operation is allowed, information can be permanently stored with the clock line in either the low or high state. The CD4031B has a MODE CONTROL input that, when in the high state, allows operation in the recirculating mode. The MODE CONTROL input can also be used to select between two separate data sources. Register packages can be cascaded and the clock lines driven directly for high-speed operation. Alternatively, a delayed clock output (CL_D) is provided that enables cascading register packages while allowing reduced clock drive fan-out and transition-time requirements. A third cascading option makes use of the Q' output from the 1/2 stage, which is available on the next negative-going transition of the clock after the Q output occurs. This delayed output, like the delayed clock CL_D, is used with clocks having slow rise and fall times.

The CD4031B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

MAXIMUM RATINGS, Absolute-Maximum Values:

| | |
|---|-------------------------------------|
| DC SUPPLY-VOLTAGE RANGE, (V _{DD}) | -0.5V to +20V |
| Voltages referenced to V _{SS} Terminal) | |
| INPUT VOLTAGE RANGE, ALL INPUTS | -0.5V to V _{DD} +0.5V |
| DC INPUT CURRENT, ANY ONE INPUT | ±10mA |
| POWER DISSIPATION PER PACKAGE (P _D): | |
| For T _A = -55°C to +100°C | 500mW |
| For T _A = +100°C to +125°C | Derate Linearly at 12mW/°C to 200mW |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR | |
| FOR T _A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) | 100mW |
| OPERATING-TEMPERATURE RANGE (T _A) | -55°C to +125°C |
| STORAGE TEMPERATURE RANGE (T _{stg}) | -65°C to +150°C |
| LEAD TEMPERATURE (DURING SOLDERING): | |
| At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max | +265°C |

Features:

- Fully static operation: DC to 12 MHz typ. @ V_{DD}-V_{SS} = 15 V
- Standard TTL drive capability on Q output
- Recirculation capability
- Three cascading modes:
 - Direct clocking for high-speed operation
 - Delayed clocking for reduced clock drive requirements
 - Additional 1/2 stage for slow clocks
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range)

| |
|---------------------------------|
| 1 V at V _{DD} = 5 V |
| 2 V at V _{DD} = 10 V |
| 2.5 V at V _{DD} = 15 V |

- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

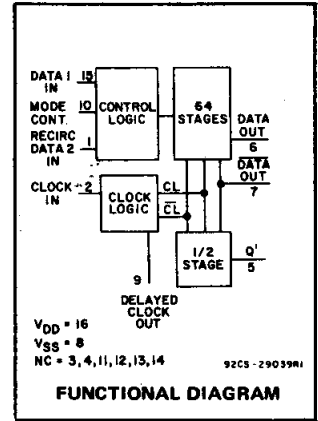
Applications:

- Serial shift registers
- Time delay circuits

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC | LIMITS | | UNITS |
|---|--------|------|-------|
| | Min. | Max. | |
| Supply-Voltage Range (For T _A =Full Package-Temperature Range) | 3 | 18 | V |



INPUT CONTROL CIRCUIT TRUTH TABLE

| DATA | RECIRC. | MODE | BIT INTO STAGE 1 |
|------|---------|------|------------------|
| 1 | X | 0 | 1 |
| 0 | X | 0 | 0 |
| X | 1 | 1 | 1 |
| X | 0 | 1 | 0 |

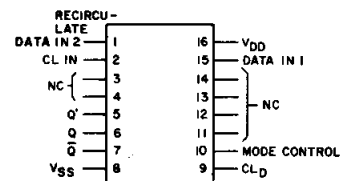
TYPICAL STAGE TRUTH TABLE

| Data | CL | Data + 1 |
|------|----|----------|
| 0 | | 0 |
| 1 | | 1 |
| X | | NC |

TRUTH TABLE FOR OUTPUT FROM Q' (TERMINAL 5)

| Data + 64 | CL | Data + 64½ |
|-----------|----|------------|
| 0 | | 0 |
| 1 | | 1 |
| X | | NC |

1 = HIGH LEVEL 0 = LOW LEVEL
X = DON'T CARE NC = NO CHANGE



TERMINAL ASSIGNMENT

3
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HIGH VOLTAGE ICs

CD4031B Types

STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|---|--------------------|---------------------|---------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
| | V _O (V) | V _{IN} (V) | V _{DD} (V) | -55 | -40 | +85 | +125 | +25 | | | |
| | | | | | | | | Min. | Typ. | Max. | |
| Quiescent Device Current, I _{DD} Max. | — | 0.5 | 5 | 5 | 5 | 150 | 150 | — | 0.04 | 5 | μA |
| | — | 0.10 | 10 | 10 | 10 | 300 | 300 | — | 0.04 | 10 | |
| | — | 0.15 | 15 | 20 | 20 | 600 | 600 | — | 0.04 | 20 | |
| | — | 0.20 | 20 | 100 | 100 | 3000 | 3000 | — | 0.08 | 100 | |
| Output Low (Sink) Current I _{OL} Min. Q | 0.4 | 0.5 | 5 | 2.56 | 2.44 | 1.68 | 1.44 | 2.04 | 4 | — | mA |
| | 0.5 | 0.10 | 10 | 6.4 | 6 | 4.4 | 3.6 | 5.2 | 10.4 | — | |
| | 1.5 | 0.15 | 15 | 16.8 | 16 | 11.2 | 9.6 | 13.6 | 27.2 | — | |
| Q̄, Q', CL _D | 0.4 | 0.5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | — | mA |
| | 0.5 | 0.10 | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | — | |
| | 1.5 | 0.15 | 15 | 4.2 | 4 | 2.8 | 2.4 | 3.4 | 6.8 | — | |
| Output High (Source) Current, I _{OH} Min. Q, Q̄, Q', CL _D | 4.6 | 0.5 | 5 | -0.64 | -0.61 | -0.42 | -0.36 | -0.51 | -1 | — | mA |
| | 2.5 | 0.5 | 5 | -2 | -1.8 | -1.3 | -1.15 | -1.6 | -3.2 | — | |
| | 9.5 | 0.10 | 10 | -1.6 | -1.5 | -1.1 | -0.9 | -1.3 | -2.6 | — | |
| Output Voltage: Low-Level, V _{OL} Max. | — | 0.5 | 5 | — | — | 0.05 | — | — | 0 | 0.05 | V |
| | — | 0.10 | 10 | — | — | 0.05 | — | — | 0 | 0.05 | |
| | — | 0.15 | 15 | — | — | 0.05 | — | — | 0 | 0.05 | |
| Output Voltage: High-Level, V _{OH} Min. | — | 0.5 | 5 | — | — | 4.95 | — | 4.95 | 5 | — | V |
| | — | 0.10 | 10 | — | — | 9.95 | — | 9.95 | 10 | — | |
| | — | 0.15 | 15 | — | — | 14.95 | — | 14.95 | 15 | — | |
| Input Low Voltage, V _{IL} Max. | 0.5, 4.5 | — | 5 | — | — | 1.5 | — | — | — | 1.5 | V |
| | 1.9 | — | 10 | — | — | 3 | — | — | — | 3 | |
| | 1.5, 13.5 | — | 15 | — | — | 4 | — | — | — | 4 | |
| Input High Voltage, V _{IH} Min. | 0.5, 4.5 | — | 5 | — | — | 3.5 | — | 3.5 | — | — | V |
| | 1.9 | — | 10 | — | — | 7 | — | 7 | — | — | |
| | 1.5, 13.5 | — | 15 | — | — | 11 | — | 11 | — | — | |
| Input Current I _{IN} Max. | — | 0.18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | — | ±10 ⁻⁵ | ±0.1 | μA |

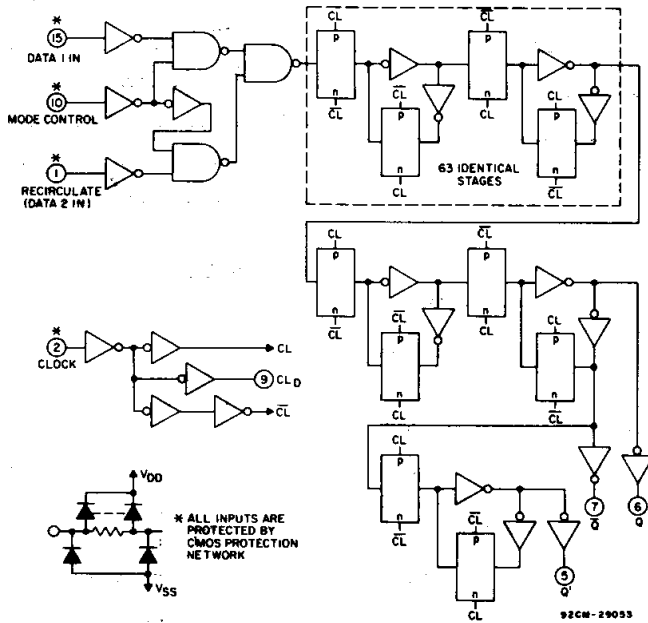


Fig. 1 - Logic diagram.

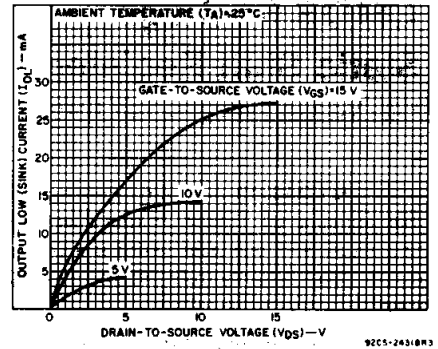


Fig. 2 - Typical output low (sink) current characteristics (Q sink current = 4X ordinate).

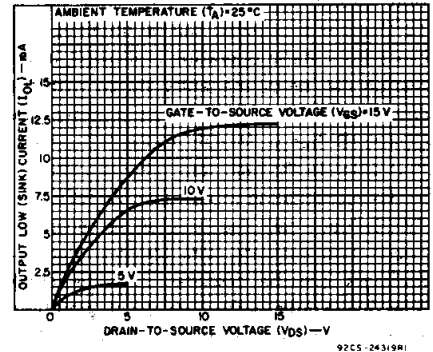


Fig. 3 - Minimum output low (sink) current characteristics (Q sink current = 4X ordinate).

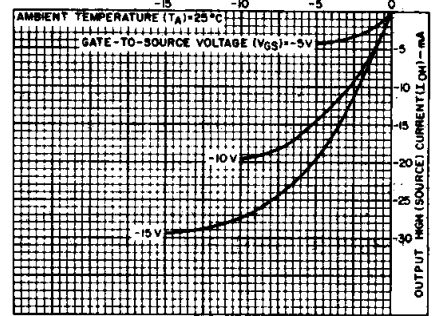


Fig. 4 - Typical output high (source) current characteristics.

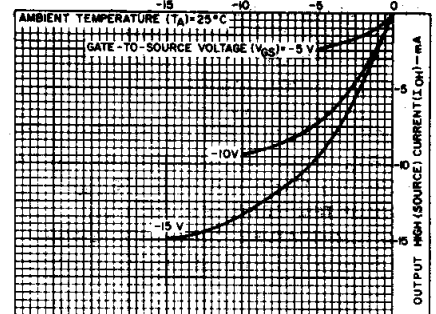


Fig. 5 - Minimum output high (source) current characteristics.

CD4031B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$; Input $t_r, t_f = 20\text{ ns}$,
 $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

| CHARACTERISTIC | TEST CONDITIONS | LIMITS | | | UNITS |
|--|-----------------|--------|------|------|---------------|
| | V_{DD} (V) | Min. | Typ. | Max. | |
| Propagation Delay Time: Clock to \bar{Q} , t_{PHL} , t_{PLH} ; Clock to Q, t_{PLH} | 5 | — | 250 | 500 | ns |
| | 10 | — | 110 | 220 | |
| | 15 | — | 90 | 180 | |
| \bar{Q} to Q' , t_{PHL} , t_{PLH} ; Clock to Q, t_{PHL} | 5 | — | 190 | 380 | ns |
| | 10 | — | 80 | 160 | |
| | 15 | — | 65 | 130 | |
| Clock to CL_D | 5 | — | 100 | 200 | ns |
| | 10 | — | 50 | 100 | |
| | 15 | — | 40 | 80 | |
| Transition Time, t_{THL} , t_{TLH} (Any Output, except Q, t_{THL}) | 5 | — | 100 | 200 | ns |
| | 10 | — | 50 | 100 | |
| | 15 | — | 40 | 80 | |
| Q, t_{THL} | 5 | — | 50 | 100 | ns |
| | 10 | — | 25 | 50 | |
| | 15 | — | 20 | 40 | |
| Minimum Data Setup Time, t_S | 5 | — | 30 | 60 | ns |
| | 10 | — | 15 | 30 | |
| | 15 | — | 10 | 20 | |
| Minimum Data Hold Time, t_H | 5 | — | 30 | 60 | ns |
| | 10 | — | 15 | 30 | |
| | 15 | — | 10 | 20 | |
| Minimum Clock Pulse Width, t_W | 5 | — | 120 | 240 | ns |
| | 10 | — | 50 | 100 | |
| | 15 | — | 40 | 80 | |
| Maximum Clock Input Frequency, f_{CL}^{**} | 5 | 2 | 4 | — | MHz |
| | 10 | 5 | 10 | — | |
| | 15 | 6 | 12 | — | |
| Clock Input Rise or Fall Time, t_{rCL} , t_{fCL}^* | 5 | — | — | 1000 | μs |
| | 10 | — | — | 1000 | |
| | 15 | — | — | 200 | |
| Input Capacitance, C_{IN} (Any Input) | — | — | 5 | 7.5 | pF |

*If more than one unit is cascaded in the parallel clocked application, t_{rCL} should be made less than or equal to the sum of the propagation delay at 50 pF and the transition time of the output driving stage.

**Maximum Clock Frequency for Cascaded Units;

a) Using Delayed Clock Feature in Recirculation Mode:

$$f_{max} = \frac{1}{(n-1) C_{LD} \text{ prop. delay} + Q \text{ prop. delay} + \text{set-up time}}$$

where n = number of packages

b) Not Using Delayed Clock:

$$f_{max} = \frac{1}{\text{propagation delay} + \text{set-up time}}$$

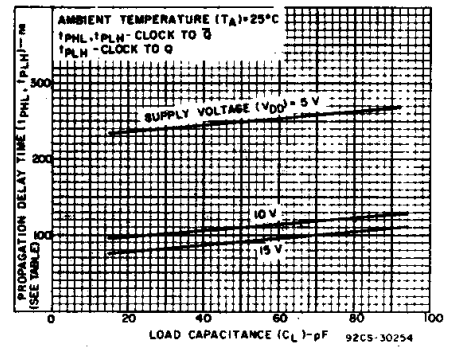


Fig. 6 — Typical propagation delay time as a function of load capacitance (see table).

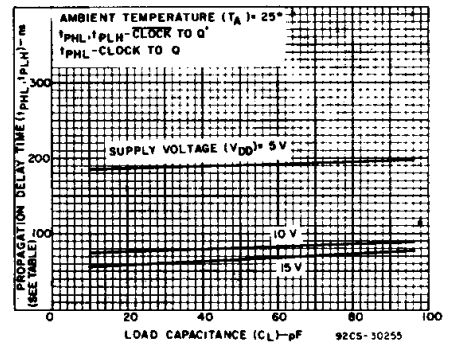


Fig. 7 — Typical propagation delay time as a function of load capacitance (see table).

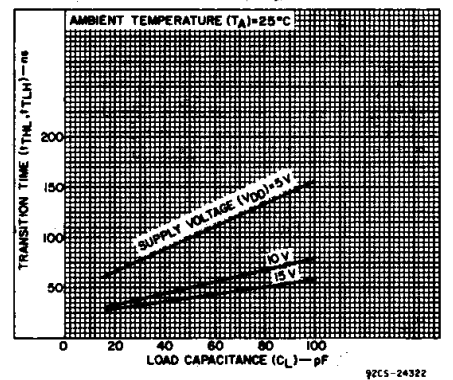


Fig. 8 — Typical transition time as a function of load capacitance (except Q, t_{THL}).

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HIGH VOLTAGE ICs

CD4031B Types

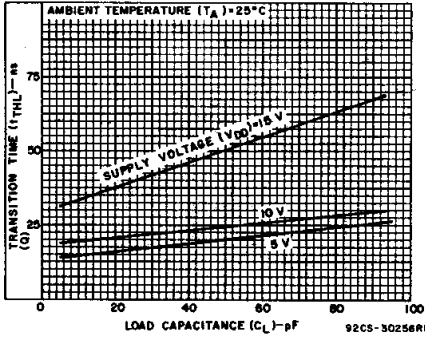


Fig. 9 - Typical transition time as a function of load capacitance (Q , t_{THL}).

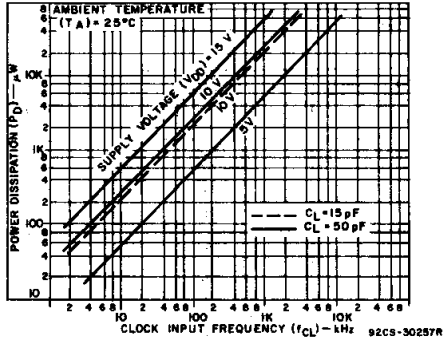


Fig. 10 - Typical dynamic power dissipation as a function of clock input frequency.

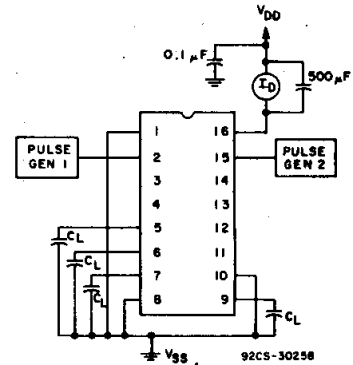


Fig. 11 - Dynamic power dissipation test circuit.
NOTE: P.G.1 = f_{CL} ; P.G.2 = $\frac{f_{CL}}{4}$

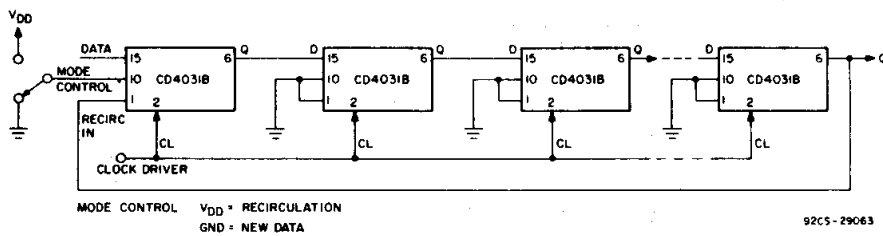


Fig. 12 - Cascading using direct clocking for high-speed operation (see clock rise and fall time requirement).

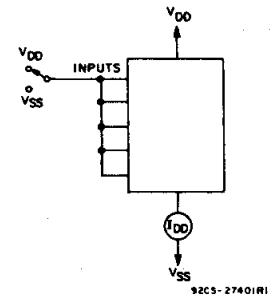


Fig. 13 - Quiescent device current test circuit.

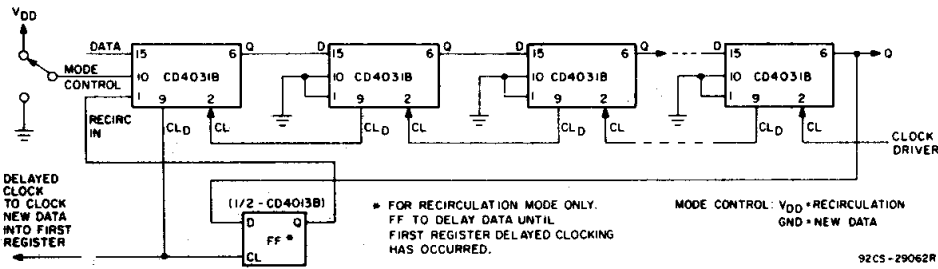


Fig. 14 - Cascading using delayed clocking for reduced clock drive requirements.

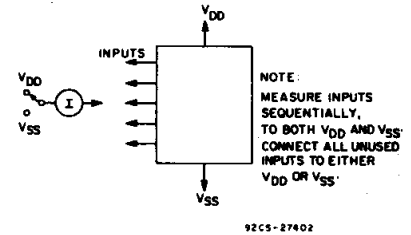


Fig. 15 - Input-leakage current.

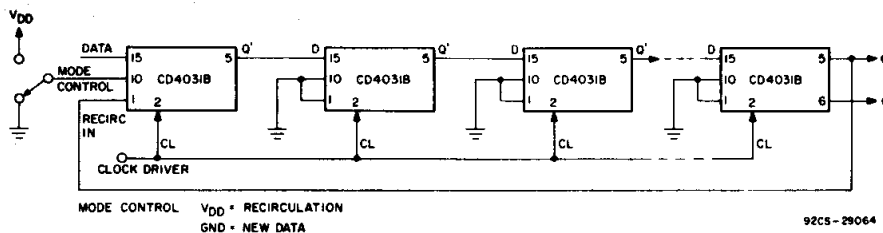


Fig. 16 - Cascading using half-clock-pulse delayed data output (Q') to permit use of slow rise and fall time clock inputs.

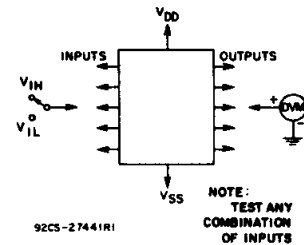
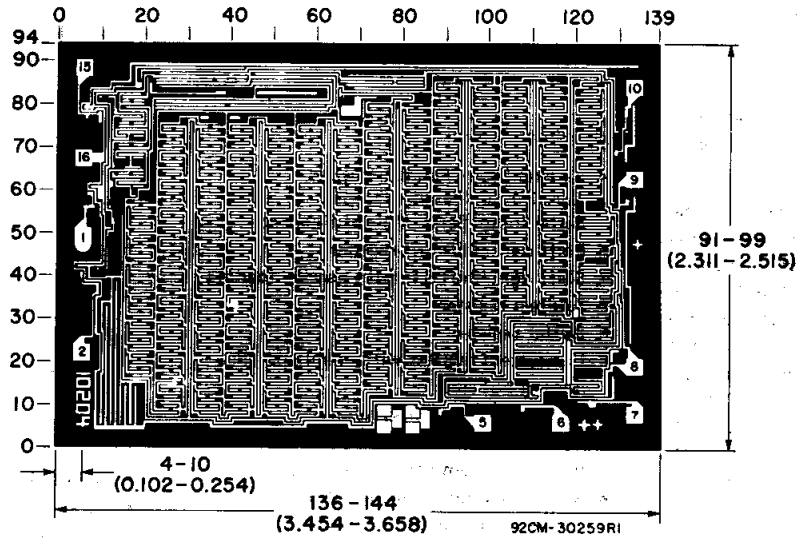


Fig. 17 - Input-voltage test circuit.

CD4031B Types



Chip dimensions and pad layout for CD4031B

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

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PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| CD4031BE | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| CD4031BF3A | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| CD4031BNSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4031BNSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4031BPW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4031BPWE4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4031BPWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4031BPWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

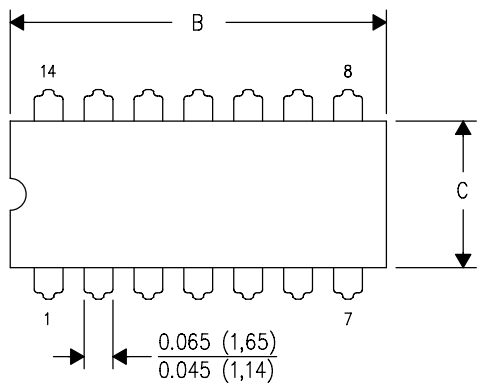
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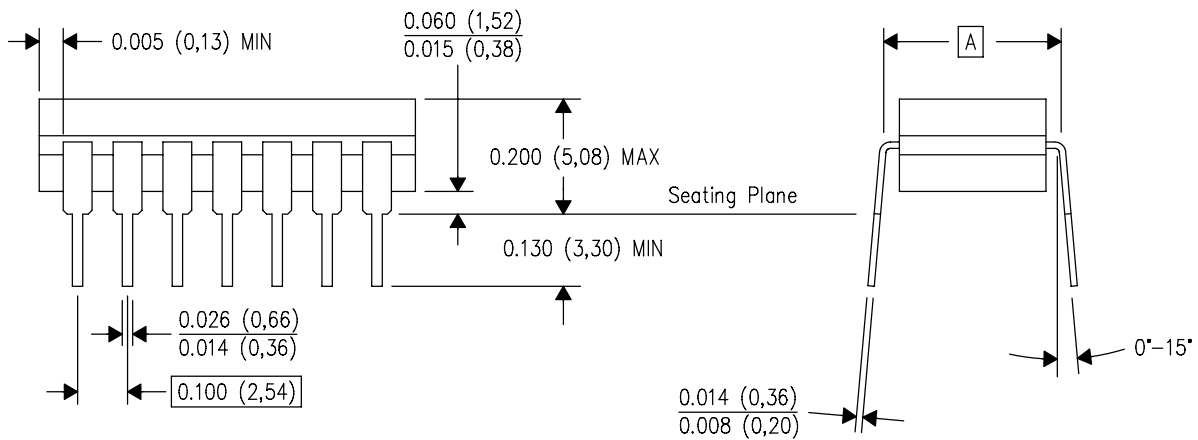
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



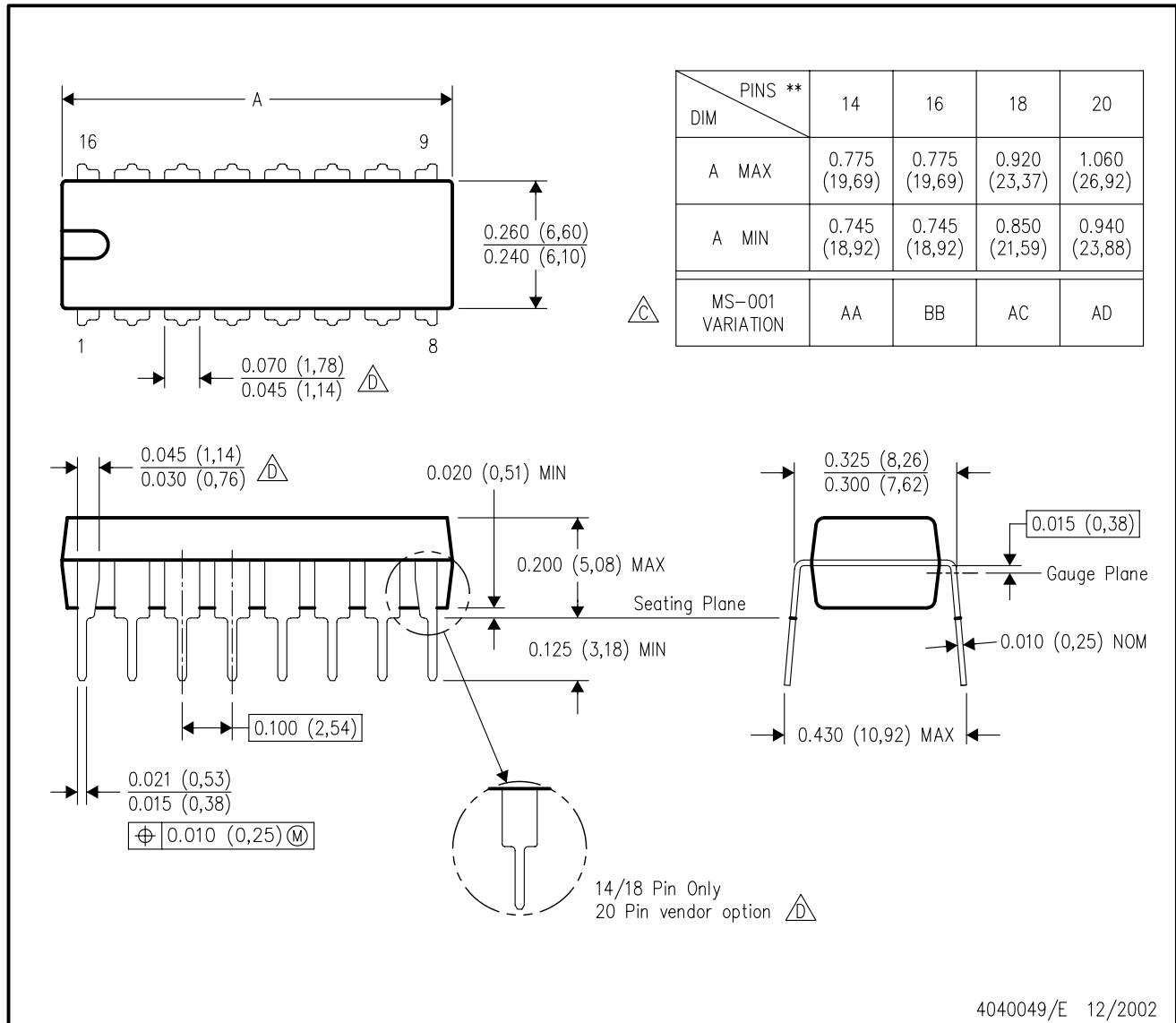
4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



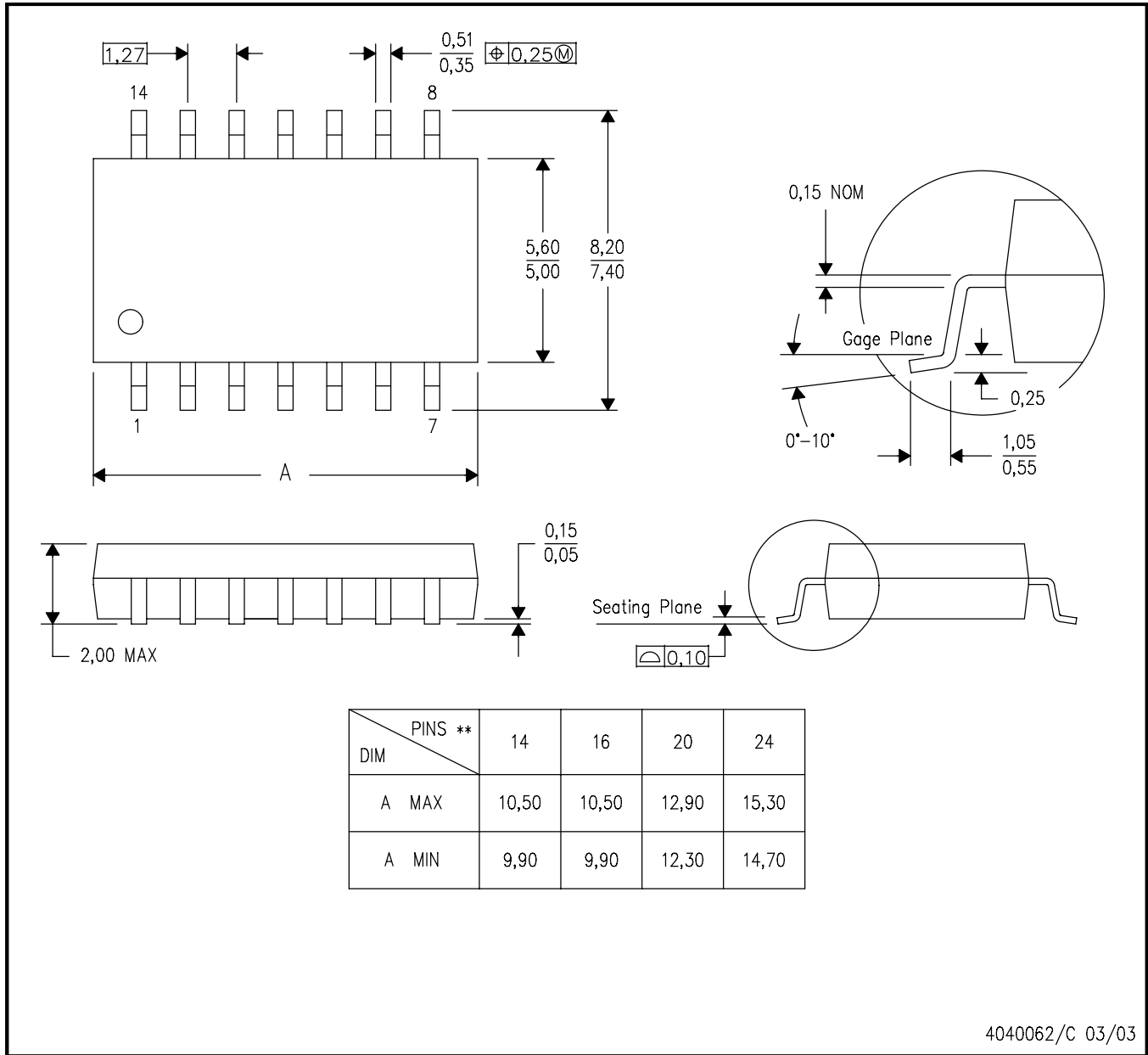
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

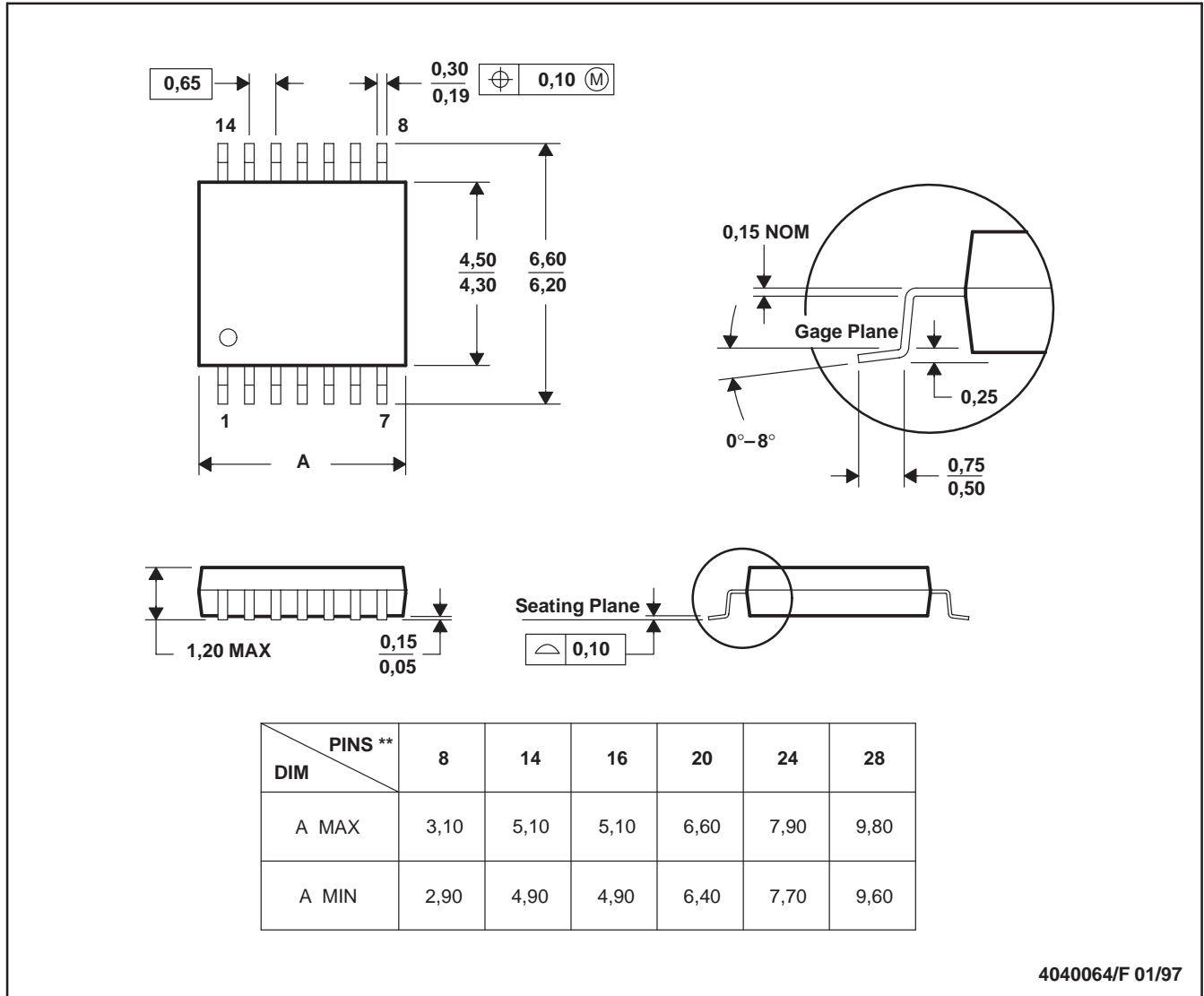


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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