TPA3113D2 6-W Filter-Free Stereo Class-D Audio Power Amplifier With SpeakerGuard™

1 Features

- 6-W/ch into an 8-Ω Loads at 10% THD+N From a 10-V Supply
- 12-W into a 4-Ω Mono Load at 10% THD+N From a 10-V Supply
- 87% Efficient Class-D Operation Eliminates Need for Heat Sinks
- Wide Supply Voltage Range Allows Operation from 8 V to 26 V
- Filter-Free Operation
- SpeakerGuard™ Speaker Protection Includes Adjustable Power Limiter Plus DC Protection
- Flow-Through Pinout Facilitates Easy Board Layout
- Robust Pin-to-Pin Short-Circuit Protection and Thermal Protection With Auto Recovery Option
- Excellent THD+N and Pop-Free Performance
- Four Selectable, Fixed Gain Settings
- Differential Inputs

2 Applications

- Televisions
- Consumer Audio Equipment
- Monitors

3 Description

The TPA3113D2 is a 6-W (per channel) efficient, Class-D audio power amplifier for driving bridged-tied stereo speakers. Advanced EMI Suppression Technology enables the use of inexpensive ferrite bead filters at the outputs while meeting EMC requirements. SpeakerGuard™ speaker protection circuitry includes an adjustable power limiter and a DC detection circuit. The adjustable power limiter allows the user to set a *virtual* voltage rail lower than the chip supply to limit the amount of current through the speaker. The DC detect circuit measures the frequency and amplitude of the PWM signal and shuts off the output stage if the input capacitors are damaged or shorts exist on the inputs.

The TPA3113D2 can drive stereo speakers as low as 4 Ω. The high efficiency of the TPA3113D2, 87%, eliminates the need for an external heat sink when playing music.

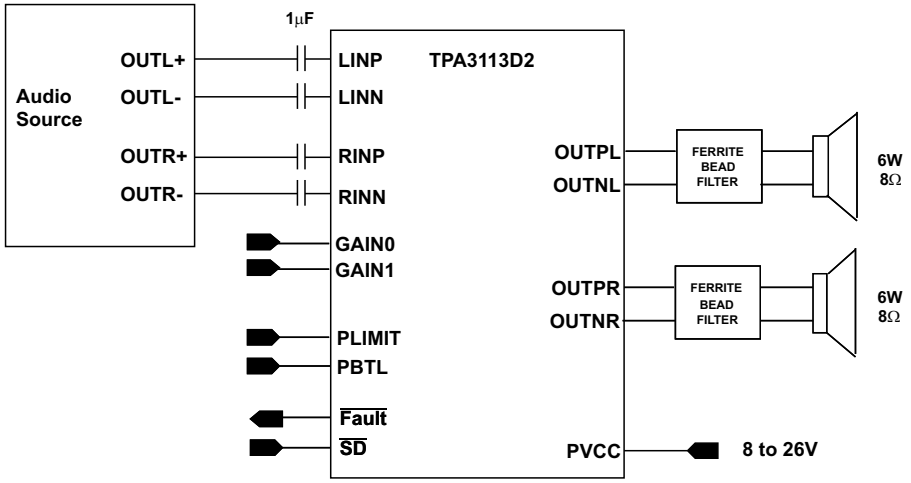
The outputs are also fully protected against shorts to GND, VCC, and output-to-output. The short-circuit protection and thermal protection includes an auto-recovery feature.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPA3113D2	TSSOP (28)	9.70 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

TPA3113D2 Simplified Application Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (July 2012) to Revision F — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Revision D (August 2010) to Revision E — **Page**

- Added < 10 V/ms to V_I in the Absolute Maximum Ratings table ... 5
- Added a 100kΩ resistor to AVCC Pin 14 and Note 1 to Figure 39 ... 25

Changes from Revision C (July 2010) to Revision D — **Page**

- Replace the Dissipations Ratings Table with the Thermal Information Table ... 6

Changes from Revision B (September 2009) to Revision C — **Page**

- Added slew rate adjustment information ... 14

Changes from Revision A (August 2009) to Revision B — **Page**

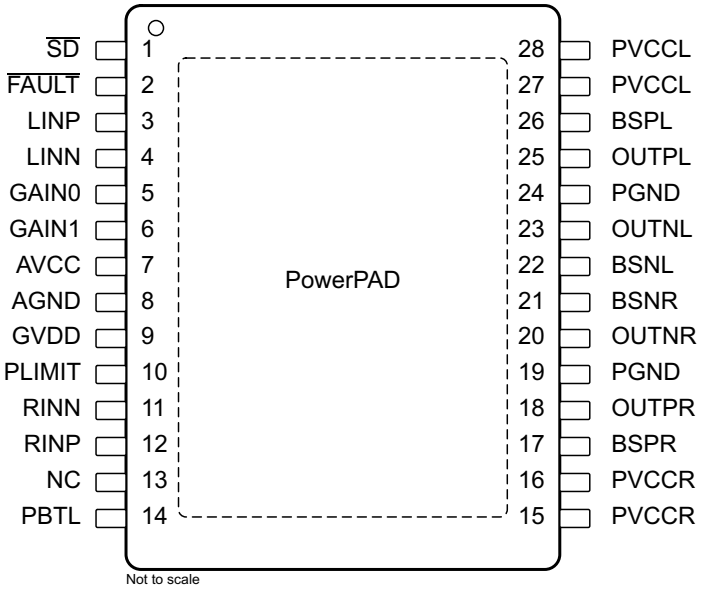
- Added the Pin out illustration. ... 4
- Changed the Stereo Class-D Amplifier with BTL Output and Single-Ended Input illustration Figure 38 - Corrected the pin names. ... 24
- Changed the Stereo Class-D Amplifier with PBTL Output and Single-Ended Input Figure 39 - Corrected the pin names. 25

Changes from Original (August 2009) to Revision A **Page**

- Changed Feature From: 90% Efficient Class-D Operation Eliminates Need for Heat Sinks To: 87% Efficient Class-D Operation Eliminates Need for Heat Sinks 1
- Changed the Drain Source TYP value From: 240 to 400 mΩ. 6
- Changed the Drain Source TYP value From: 240 to 400 mΩ. 7
- Changed AC Char 24V - P_O From: THD+N = 10%, f = 1 kHz, V_{CC} = 16 V (TYP = 15W) To: THD+N = 10%, f = 1 kHz, V_{CC} = 10 V (TYP = 6W) 7
- Changed AC Char 24V - THD+N From: V_{CC} = 16 V, f = 1 kHz, P_O = 7.5 W (half-power) To: V_{CC} = 16 V, f = 1 kHz, P_O = 3 W (half-power) TYP From: 0.1 To: 0.07 7
- Deleted AC Char 12V -, PO - Continuous output power 7
- Changed AC Char 12V - THD+N From: V_{CC} = 16 V, f = 1 kHz, P_O = 5 W (half-power) To: V_{CC} = 16 V, f = 1 kHz, P_O = 3 W (half-power) 7
- Changed multiple graphs in the TYPICAL CHARACTERISTICS. 8

5 Pin Configuration and Functions

PWP Package
28-Pin TSSOP
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	$\overline{SD}$	I	Shutdown logic input for audio amp (LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to AVCC.
2	$\overline{FAULT}$	O	Open drain output used to display short circuit or dc detect fault status. Voltage compliant to AVCC. Short circuit faults can be set to auto-recovery by connecting $\overline{FAULT}$ pin to $\overline{SD}$ pin. Otherwise, both short circuit faults and dc detect faults must be reset by cycling PVCC.
3	LINP	I	Positive audio input for left channel. Biased at 3 V.
4	LINN	I	Negative audio input for left channel. Biased at 3 V.
5	GAIN0	I	Gain select least significant bit. TTL logic levels with compliance to AVCC.
6	GAIN1	I	Gain select most significant bit. TTL logic levels with compliance to AVCC.
7	AVCC	P	Analog supply
8	AGND	—	Analog signal ground. Connect to the thermal pad.
9	GVDD	O	High-side FET gate drive supply. Nominal voltage is 7 V. Also should be used as supply for PLIMIT function
10	PLIMIT	I	Power limit level adjust. Connect a resistor divider from GVDD to GND to set power limit. Connect directly to GVDD for no power limit.
11	RINN	I	Negative audio input for right channel. Biased at 3 V.
12	RINP	I	Positive audio input for right channel. Biased at 3 V.
13	NC	—	Not connected
14	PBTL	I	Parallel BTL mode switch
15	PVCCR	P	Power supply for right channel H-bridge. Right channel and left channel power supply inputs are connect internally.
16	PVCCR	P	Power supply for right channel H-bridge. Right channel and left channel power supply inputs are connect internally.
17	BSPR	I	Bootstrap I/O for right channel, positive high-side FET.
18	OUTPR	O	Class-D H-bridge positive output for right channel.

(1) I = Input, O = Output, P = Power

Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
19	PGND	—	Power ground for the H-bridges.
20	OUTNR	O	Class-D H-bridge negative output for right channel.
21	BSNR	I	Bootstrap I/O for right channel, negative high-side FET.
22	BSNL	I	Bootstrap I/O for left channel, negative high-side FET.
23	OUTNL	O	Class-D H-bridge negative output for left channel.
24	PGND	—	Power ground for the H-bridges.
25	OUTPL	O	Class-D H-bridge positive output for left channel.
26	BSPL	I	Bootstrap I/O for left channel, positive high-side FET.
27	PVCCL	P	Power supply for left channel H-bridge. Right channel and left channel power supply inputs are connect internally.
28	PVCCL	P	Power supply for left channel H-bridge. Right channel and left channel power supply inputs are connect internally.
29	PowerPAD	—	Connect to ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	AVCC, PVCC	–0.3	30	V
V_I	Interface pin voltage	$\overline{SD}$, GAIN0, GAIN1, PBTL, $\overline{FAULT}$ (2)	–0.3	V_{CC} + 0.3	V
				< 10	V/ms
		PLIMIT	–0.3	GVDD + 0.3	V
		RINN, RINP, LINN, LINP	–0.3	6.3	V
	Continuous total power dissipation		See *Thermal Information*		
T_A	Operating free-air temperature		–40	85	°C
T_J	Operating junction temperature(3)		–40	150	°C
R_L	Minimum load resistance	BTL: PVCC > 15 V		4.8	Ω
		BTL: PVCC ≤ 15 V		3.2	
		PBTL		3.2	
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The voltage slew rate of these pins must be restricted to no more than 10 V/ms. For higher slew rates, use a 100-kΩ resister in series with the pins.
(3) The TPA3113D2 incorporates an exposed thermal pad on the underside of the chip. This acts as a heatsink, and it must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in the device going into thermal protection shutdown. See TI Technical Briefs *Quad Flatpack No-Lead Logic Packages* for more information about using the TSSOP thermal pad.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)(2)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(3)(4)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) In accordance with JEDEC Standard 22, Test Method A114-B.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(4) In accordance with JEDEC Standard 22, Test Method C101-A

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	PVCC, AVCC	8	26	V
V_{IH}	High-level input voltage	$\overline{SD}$, GAIN0, GAIN1, PBTL	2		V
V_{IL}	Low-level input voltage	$\overline{SD}$, GAIN0, GAIN1, PBTL		0.8	V
V_{OL}	Low-level output voltage	$\overline{FAULT}$, R_{PULLUP} = 100k, V_{CC} = 26 V		0.8	V
I_{IH}	High-level input current	$\overline{SD}$, GAIN0, GAIN1, PBTL, V_I = 2 V, V_{CC} = 18 V		50	μA
I_{IL}	Low-level input current	$\overline{SD}$, GAIN0, GAIN1, PBTL, V_I = 0.8 V, V_{CC} = 18 V		5	μA
T_A	Operating free-air temperature		–40	85	°C

6.4 Thermal Information

THERMAL METRIC[1][2]		TPA3113D2 PWP (TSSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the application report *Semiconductor and IC Package Thermal Metrics*.
(2) For thermal estimates of this device based on PCB copper area, see the PCB Thermal Calculator.

6.5 DC Electrical Characteristics, V_{CC} = 24 V

T_A = 25°C, V_{CC} = 24 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	Class-D output offset voltage (measured differentially)	V_I = 0 V, Gain = 36 dB			1.5	15	mV
I_{CC}	Quiescent supply current	$\overline{SD}$ = 2 V, no load, PV_{CC} = 24 V			32	50	mA
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	$\overline{SD}$ = 0.8 V, no load, PV_{CC} = 24 V			250	400	μA
$r_{DS(on)}$	Drain-source ON-state resistance	V_{CC} = 12 V, I_O = 500 mA, T_J = 25°C	High Side		400		mΩ
			Low side		400		
G	Gain	GAIN1 = 0.8 V	GAIN0 = 0.8 V	19	20	21	dB
			GAIN0 = 2 V	25	26	27	
		GAIN1 = 2 V	GAIN0 = 0.8 V	31	32	33	dB
			GAIN0 = 2 V	35	36	37	
t_{on}	Turnon time	$\overline{SD}$ = 2 V			14		ms
t_{OFF}	Turnoff time	$\overline{SD}$ = 0.8 V			2		μs
GVDD	Gate Drive Supply	I_{GVDD} = 100 μA		6.4	6.9	7.4	V
t_{DCDET}	DC Detect time	$V_{(RINN)}$ = 6 V, VRINP = 0 V			420		ms

6.6 DC Electrical Characteristics, V_{CC} = 12 V

T_A = 25°C, V_{CC} = 12 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
| V_{OS} |	Class-D output offset voltage (measured differentially)	V_I = 0 V, Gain = 36 dB			1.5	15	mV
I_{CC}	Quiescent supply current	$\overline{SD}$ = 2 V, no load, PV_{CC} = 12 V			20	35	mA
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	$\overline{SD}$ = 0.8 V, no load, PV_{CC} = 12 V			200		µA
$r_{DS(on)}$	Drain-source ON-state resistance	V_{CC} = 12 V, I_O = 500 mA, T_J = 25°C	High Side		400		mΩ
			Low side		400		
G	Gain	GAIN1 = 0.8 V	GAIN0 = 0.8 V	19	20	21	dB
			GAIN0 = 2 V	25	26	27	
		GAIN1 = 2 V	GAIN0 = 0.8 V	31	32	33	dB
			GAIN0 = 2 V	35	36	37	
t_{ON}	Turnon time	$\overline{SD}$ = 2 V			14		ms
t_{OFF}	Turnoff time	$\overline{SD}$ = 0.8 V			2		µs
GVDD	Gate Drive Supply	I_{GVDD} = 2 mA		6.4	6.9	7.4	V
V_O	Output Voltage maximum under PLIMIT control	$V_{(PLIMIT)}$ = 2 V; V_I = 1 Vrms		6.75	7.90	8.75	V

6.7 AC Electrical Characteristics, V_{CC} = 24 V

T_A = 25°C, V_{CC} = 24 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
K_{SVR}	Power Supply ripple rejection	200 mV_{PP} ripple at 1 kHz, Gain = 20 dB, Inputs AC-coupled to AGND		–70		dB
P_O	Continuous output power	THD+N = 10%, f = 1 kHz, V_{CC} = 10 V		6		W
THD+N	Total harmonic distortion + noise	V_{CC} = 16 V, f = 1 kHz, P_O = 3 W (half-power)		0.07%		
V_n	Output integrated noise	20 Hz to 22 kHz, A-weighted filter, Gain = 20 dB		65		µV
				–80		dBV
	Crosstalk	V_O = 1 Vrms, Gain = 20 dB, f = 1 kHz		–100		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1 kHz, Gain = 20 dB, A-weighted		102		dB
f_{OSC}	Oscillator frequency		250	310	350	kHz
	Thermal trip point			150		°C
	Thermal hysteresis			15		°C

6.8 AC Electrical Characteristics, V_{CC} = 12 V

T_A = 25°C, V_{CC} = 12 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
K_{SVR}	Supply ripple rejection	200 mV_{PP} ripple from 20 Hz–1 kHz, Gain = 20 dB, Inputs AC-coupled to AGND		–70		dB
THD+N	Total harmonic distortion + noise	R_L = 8 Ω, f = 1 kHz, P_O = 3 W (half-power)		0.06%		
V_n	Output integrated noise	20 Hz to 22 kHz, A-weighted filter, Gain = 20 dB		65		µV
				–80		dBV
	Crosstalk	P_o = 1 W, Gain = 20 dB, f = 1 kHz		–100		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1 kHz, Gain = 20 dB, A-weighted		102		dB
f_{OSC}	Oscillator frequency		250	310	350	kHz
	Thermal trip point			150		°C
	Thermal hysteresis			15		°C

6.9 Typical Characteristics

(All Measurements taken at 1 kHz, unless otherwise noted. Measurements were made using the TPA3113D2 EVM which is available at ti.com.)

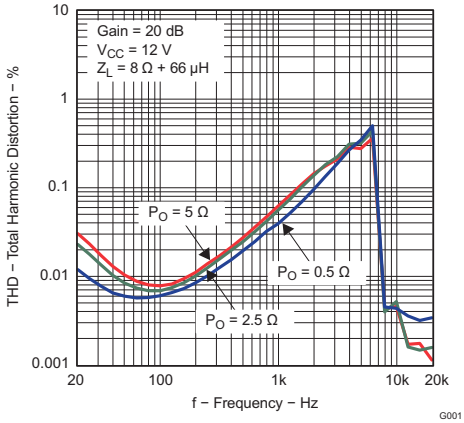


Figure 1. Total Harmonic Distortion vs Frequency (BTL)

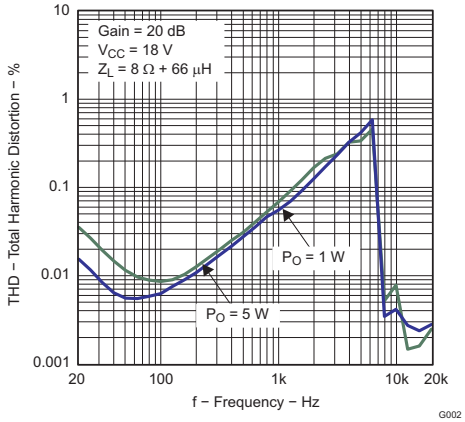


Figure 2. Total Harmonic Distortion vs Frequency (BTL)

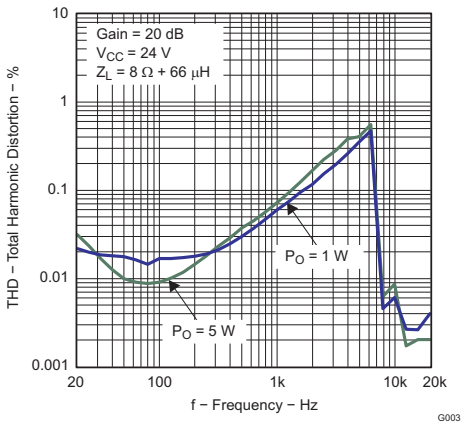


Figure 3. Total Harmonic Distortion vs Frequency (BTL)

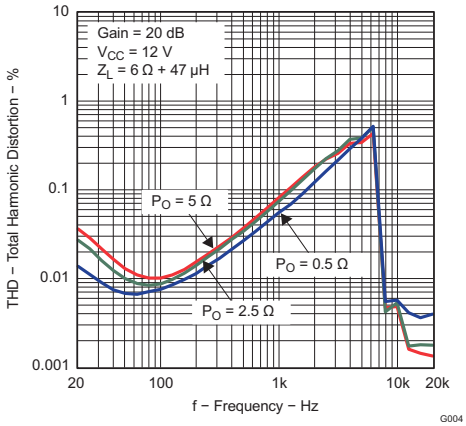


Figure 4. Total Harmonic Distortion vs Frequency (BTL)

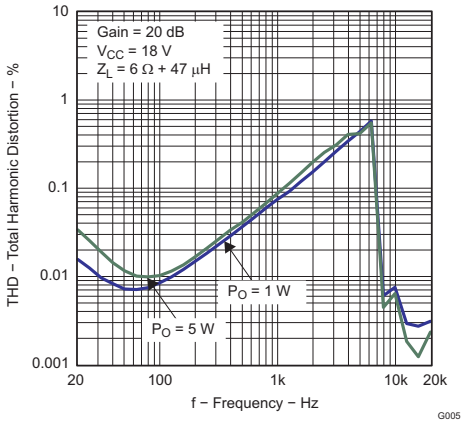


Figure 5. Total Harmonic Distortion vs Frequency (BTL)

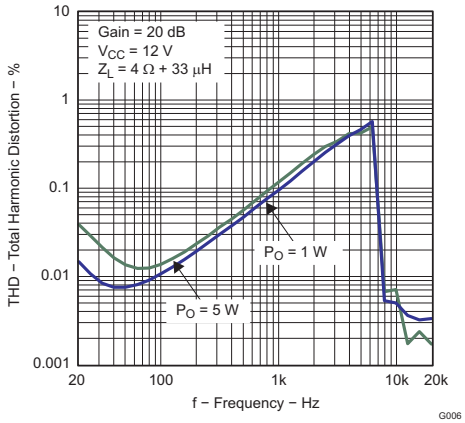


Figure 6. Total Harmonic Distortion vs Frequency (BTL)

Typical Characteristics (continued)

(All Measurements taken at 1 kHz, unless otherwise noted. Measurements were made using the TPA3113D2 EVM which is available at ti.com.)

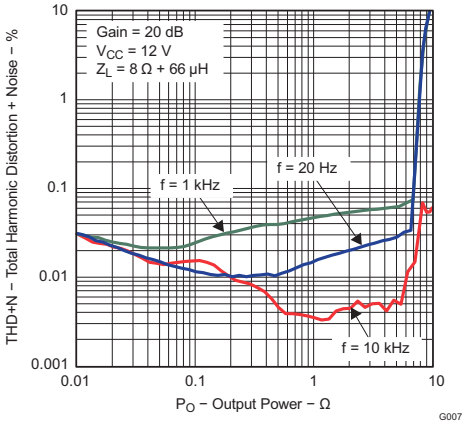


Figure 7. Total Harmonic Distortion + Noise vs Output Power (BTL)

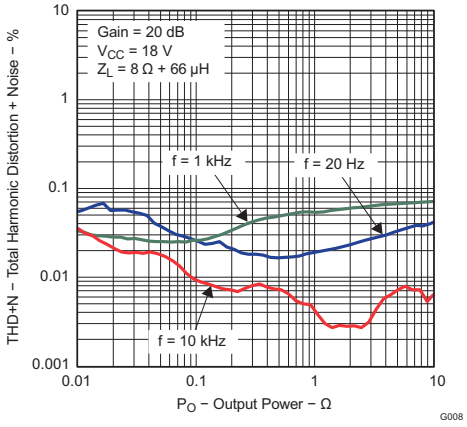


Figure 8. Total Harmonic Distortion + Noise vs Output Power (BTL)

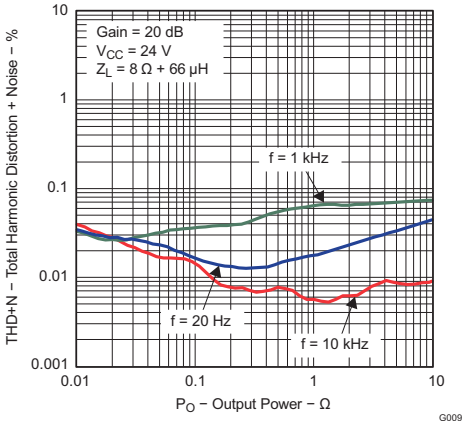


Figure 9. Total Harmonic Distortion + Noise vs Output Power (BTL)

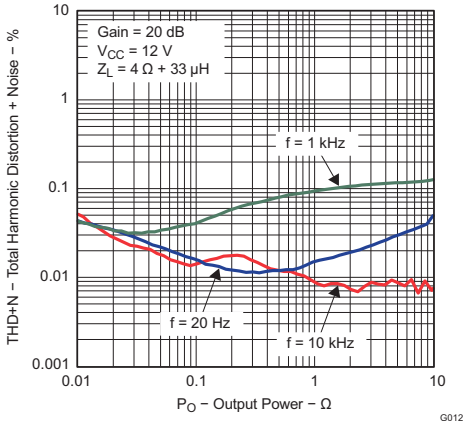
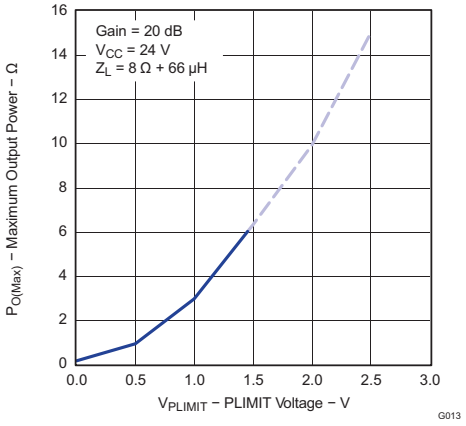
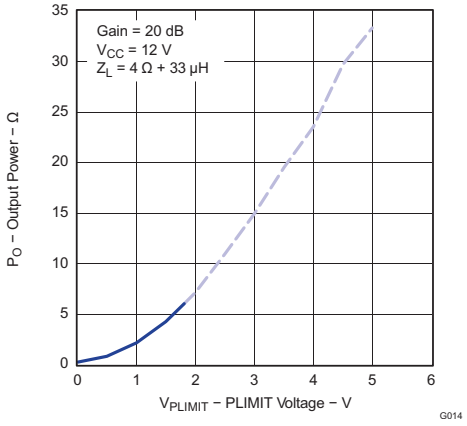


Figure 10. Total Harmonic Distortion + Noise vs Output Power (BTL)



Dashed line represents thermally limited region.

Figure 11. Maximum Output Power vs PLIMIT Voltage (BTL)



Dashed line represents thermally limited region.

Figure 12. Output Power vs PLIMIT Voltage (BTL)

Typical Characteristics (continued)

(All Measurements taken at 1 kHz, unless otherwise noted. Measurements were made using the TPA3113D2 EVM which is available at ti.com.)

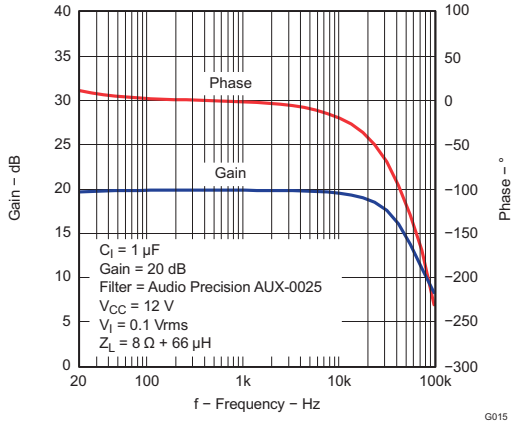
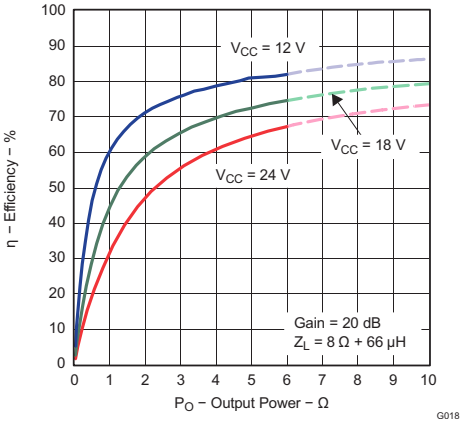
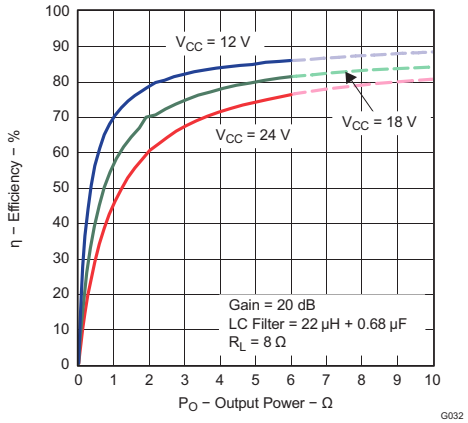


Figure 13. Gain/Phase vs Frequency (BTL)



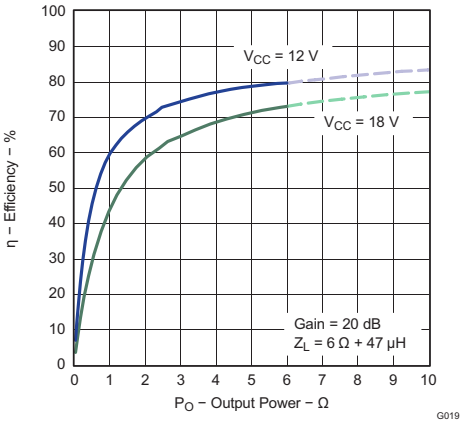
Dashed lines represent thermally limited region.

Figure 14. Efficiency vs Output Power (BTL)



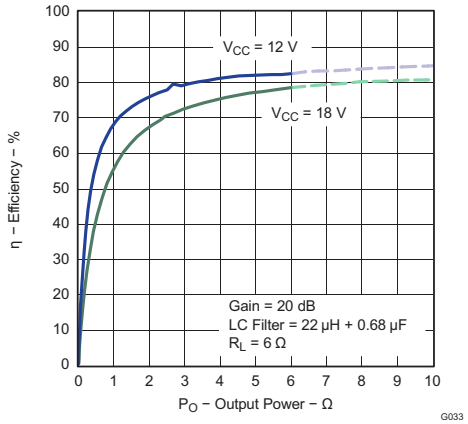
Dashed lines represent thermally limited region.

Figure 15. Efficiency vs Output Power (BTL With LC Filter)



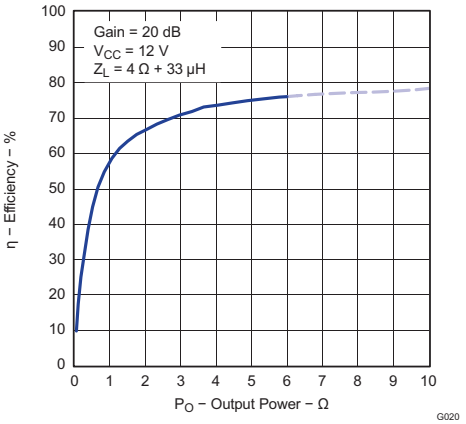
Dashed lines represent thermally limited region.

Figure 16. Efficiency vs Output Power (BTL)



Dashed lines represent thermally limited region.

Figure 17. Efficiency vs Output Power (BTL With LC Filter)

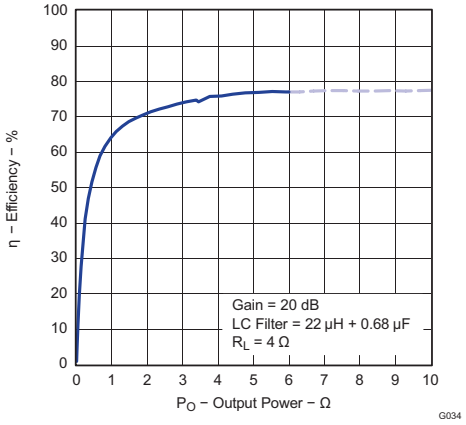


Dashed lines represent thermally limited region.

Figure 18. Efficiency vs Output Power (BTL)

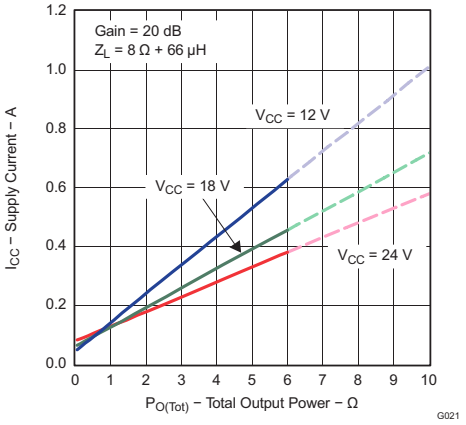
Typical Characteristics (continued)

(All Measurements taken at 1 kHz, unless otherwise noted. Measurements were made using the TPA3113D2 EVM which is available at ti.com.)



Dashed lines represent thermally limited region.

Figure 19. Efficiency vs Output Power (BTL With LC Filter)



Dashed lines represent thermally limited region.

Figure 20. Supply Current vs Total Output Power (BTL)

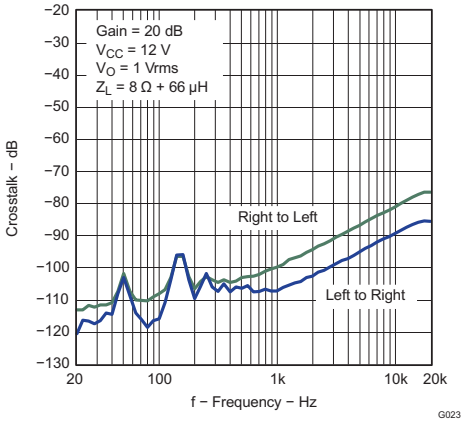


Figure 21. Crosstalk vs Frequency (BTL)

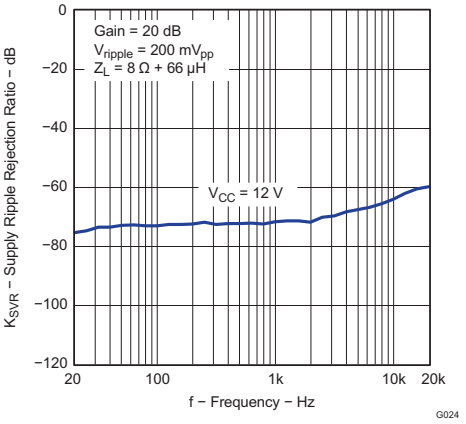


Figure 22. Supply Ripple Rejection Ratio vs Frequency (BTL)

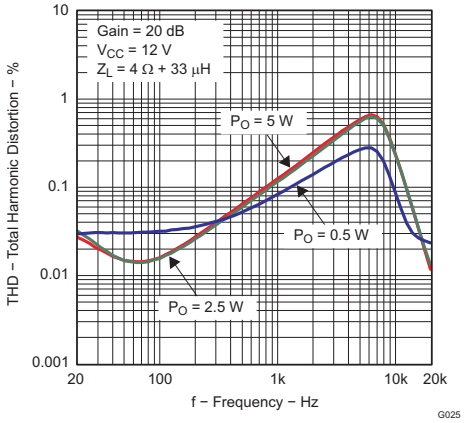


Figure 23. Total Harmonic Distortion vs Frequency (PBTL)

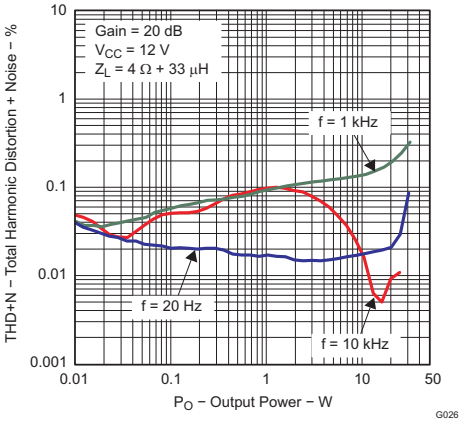


Figure 24. Total Harmonic Distortion + Noise vs Output Power (PBTL)

Typical Characteristics (continued)

(All Measurements taken at 1 kHz, unless otherwise noted. Measurements were made using the TPA3113D2 EVM which is available at ti.com.)

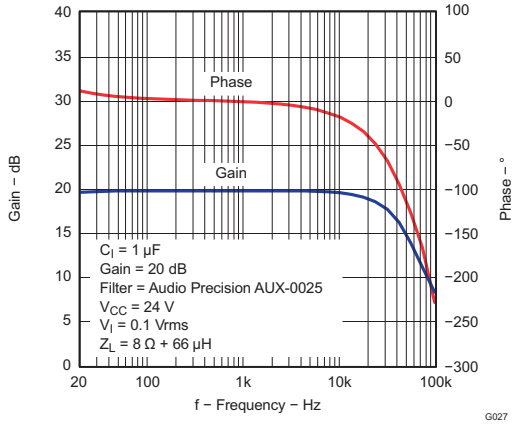


Figure 25. Gain/Phase vs Frequency (PBTL)

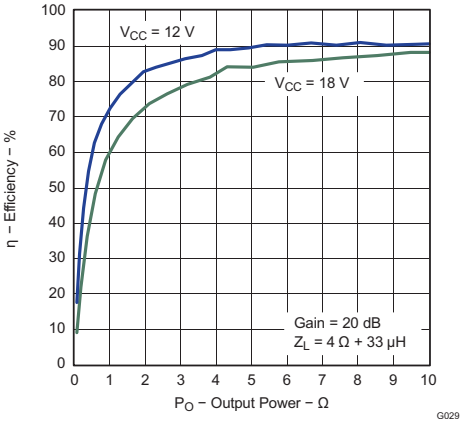


Figure 26. Efficiency vs Output Power (PBTL)

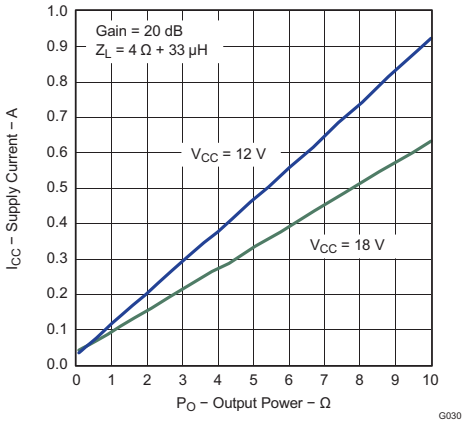


Figure 27. Supply Current vs Output Power (PBTL)

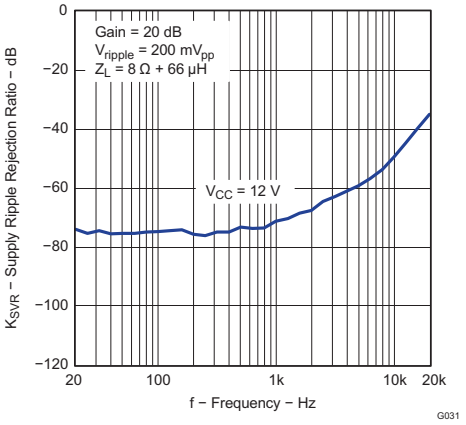


Figure 28. Supply Ripple Rejection Ratio vs Frequency (PBTL)

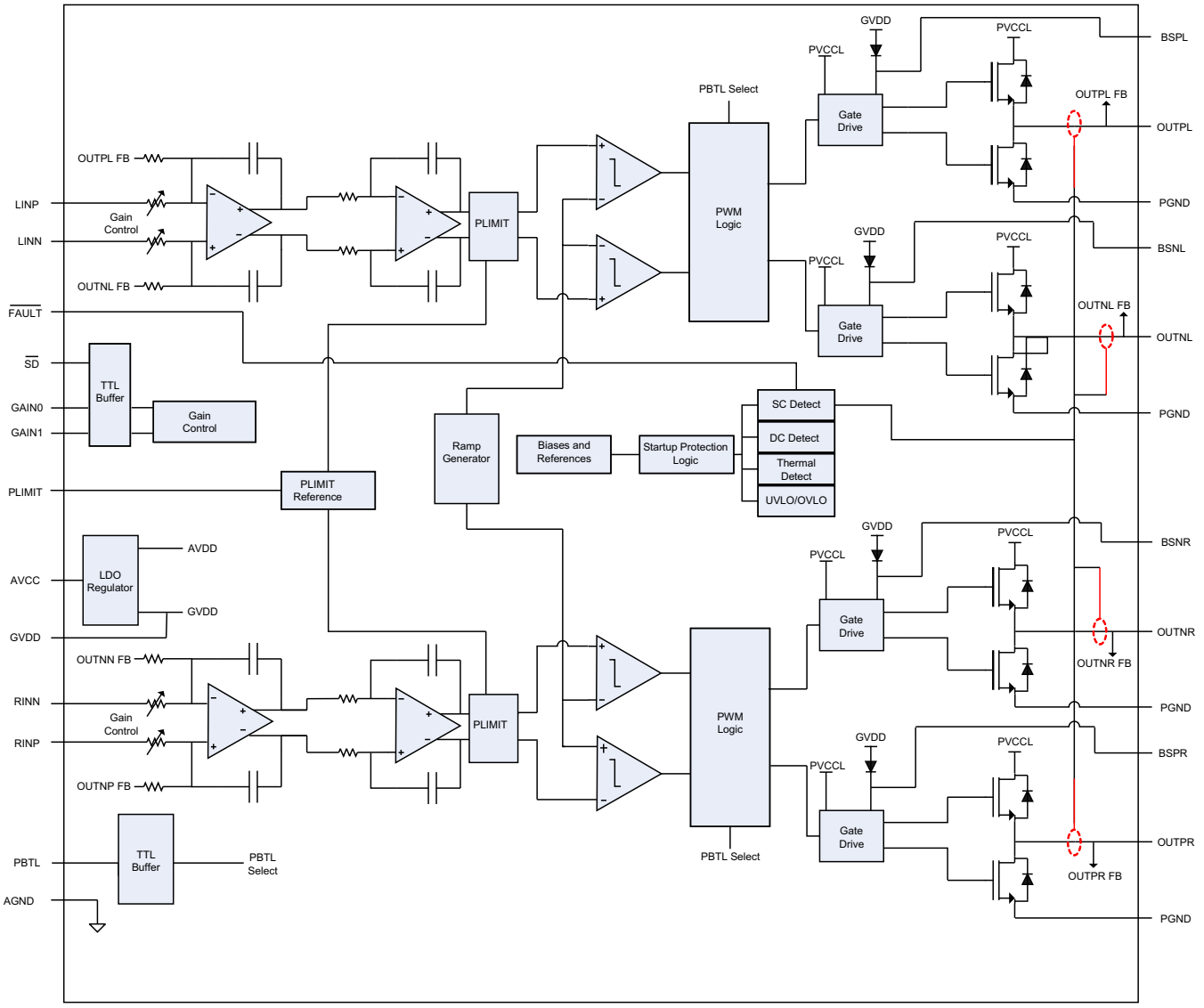
7 Detailed Description

7.1 Overview

To facilitate system design, the TPA3113D2 needs only a single power supply between 8 V and 26 V for operation. An internal voltage regulator provides suitable voltage levels for the gate driver, digital and low-voltage analog circuitry. Additionally, all circuitry requiring a floating voltage supply, that is, the high-side gate drive, is accommodated by built-in bootstrap circuitry with integrated bootstrap diodes requiring only an external capacitor for each half-bridge. The audio signal path, including the gate drive and output stage is designed as identical, independent full-bridges. Pay special attention to placing all decoupling capacitors as close to their associated pins as possible. In general, the physical loop with the power supply pins, decoupling capacitors and GND return path to the device pins must be kept as short as possible and with as little area as possible to minimize induction (see reference board documentation for additional information).

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BSXX) to the power-stage output pin (OUTXX). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD) and the bootstrap pins. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range from 310 kHz, it is recommended to use ceramic capacitors with at least 220-nF capacitance, size 0603 or 0805, for the bootstrap supply. These capacitors ensure sufficient energy storage, even during clipped low frequency audio signals, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of its ON cycle. Pay special attention to the power-stage power supply; this includes component selection, PCB placement, and routing. For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVCC pin is decoupled with ceramic capacitors placed as close as possible to each supply pin. TI recommends following the PCB layout of the TPA3113D2 reference design. For additional information on recommended power supply and required components, see the application diagrams in this data sheet. The PVCC power supply must have low output impedance and low noise. The power-supply ramp and SD release sequence is not critical for device reliability as facilitated by the internal power-on-reset circuit, but TI recommends releasing SD after the power supply is settled for minimum turnon audible artifacts.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Gain Setting Through GAIN0 and GAIN1 Inputs

The gain of the TPA3113D2 is set by two input terminals, GAIN0 and GAIN1. The voltage slew rate of these gain terminals, along with terminals 1 and 14, must be restricted to no more than 10 V/ms. For higher slew rates, use a 100-kΩ resistor in series with the terminals.

The gains listed in Table 1 are realized by changing the taps on the input resistors and feedback resistors inside the amplifier. This causes the input impedance (Z_I) to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the gain variation from part-to-part is small. However, the input impedance from part-to-part at the same gain may shift by ±20% due to shifts in the actual resistance of the input resistors.

For design purposes, the input network (discussed in the next section) should be designed assuming an input impedance of 7.2 kΩ, which is the absolute minimum input impedance of the TPA3113D2. At the lower gain settings, the input impedance could increase as high as 72 kΩ.

Table 1. Gain Setting

GAIN1	GAIN0	AMPLIFIER GAIN (dB)	INPUT IMPEDANCE (kΩ)
		TYP	TYP
0	0	20	60
0	1	26	30
1	0	32	15
1	1	36	9

7.3.2 $\overline{SD}$ Operation

The TPA3113D2 employs a shutdown mode of operation designed to reduce supply current (I_{CC}) to the absolute minimum level during periods of non-use for power conservation. The $\overline{SD}$ input terminal should be held high (see specification table for trip point) during normal operation when the amplifier is in use. Pulling $\overline{SD}$ low causes the outputs to mute and the amplifier to enter a low-current state. Never leave $\overline{SD}$ unconnected, because amplifier operation would be unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown mode prior to removing the power supply voltage.

7.3.3 PLIMIT

The voltage at pin 10 can used to limit the power to levels below that which is possible based on the supply rail. Add a resistor divider from GVDD to ground to set the voltage at the PLIMIT pin. An external reference may also be used if tighter tolerance is required. Also add a 1-μF capacitor from pin 10 to ground.

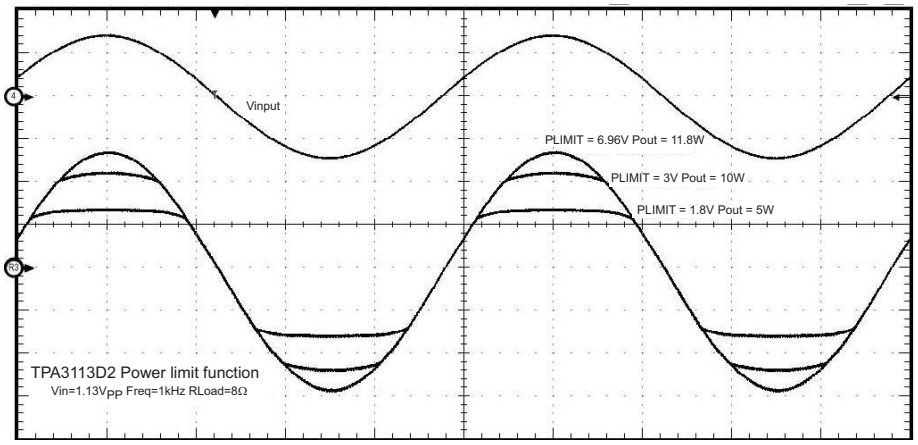


Figure 29. PLIMIT Circuit Operation

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cycle to fixed maximum value. This limit can be thought of as a *virtual* voltage rail which is lower than the supply connected to PVCC. This *virtual* rail is 4 times the voltage at the PLIMIT pin. This output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L} \quad \text{for unclipped power}$$

where

- R_S is the total series resistance including $R_{DS(on)}$, and any resistance in the output filter.
- R_L is the load resistance.
- V_P is the peak amplitude of the output possible within the supply rail.
  - $V_P = 4 \times$ PLIMIT voltage if PLIMIT $< 4 \times V_P$
  - P_{OUT} (10%THD) = 1.25 × P_{OUT} (unclipped) (1)

Table 2. PLIMIT Typical Operation

TEST CONDITIONS	PLIMIT VOLTAGE	OUTPUT POWER (W)	OUTPUT VOLTAGE AMPLITUDE (V_{P-P})
PVCC = 24 V, Vin = 1 Vrms, R_L = 8 Ω, Gain = 26 dB	1.62	5	14
PVCC = 24 V, Vin = 1 Vrms, R_L = 8 Ω, Gain = 20 dB	1.86	5	14.8
PVCC = 12 V, Vin = 1 Vrms, R_L = 8 Ω, Gain = 20 dB	1.76	5	15

7.3.4 GVDD Supply

The GVDD Supply is used to power the gates of the output full bridge transistors. It can also be used to supply the PLIMIT voltage divider circuit. Add a 1-μF capacitor to ground at this pin.

7.3.5 DC Detect

TPA3113D2 has circuitry which will protect the speakers from DC current which might occur due to defective capacitors on the input or shorts on the printed-circuit board at the inputs. A DC detect fault is reported on the $\overline{\text{FAULT}}$ pin as a low state. The DC Detect fault also causes the amplifier to shutdown by changing the state of the outputs to Hi-Z. To clear the DC Detect it is necessary to cycle the PVCC supply. Cycling $\overline{\text{S}}$ $\overline{\text{D}}$ does NOT clear a DC detect fault.

A DC Detect Fault is issued when the output differential duty-cycle of either channel exceeds 14% (for example, +57%, –43%) for more than 420 ms at the same polarity. This feature protects the speaker from large DC currents or AC currents less than 2 Hz. To avoid nuisance faults due to the DC detect circuit, hold the $\overline{\text{SD}}$ pin low at power-up until the signals at the inputs are stable. Also, take care to match the impedance seen at the positive and negative inputs to avoid nuisance DC detect faults.

The minimum differential input voltages required to trigger the DC detect are show in table 2. The inputs must remain at or above the voltage listed in the table for more than 420 ms to trigger the DC detect.

Table 3. DC Detect Threshold

AV (dB)	Vin (mV, differential)
20	112
26	56
32	28
36	17

7.3.6 PBTL Select

TPA3113D2 offers the feature of parallel BTL operation with two outputs of each channel connected directly. If the PBTL pin (pin 14) is tied high, the positive and negative outputs of each channel (left and right) are synchronized and in phase. To operate in this PBTL (mono) mode, apply the input signal to the RIGHT input and place the speaker between the LEFT and RIGHT outputs. Connect the positive and negative output together for best efficiency. For an example of the PBTL connection, see the schematic in *Application and Implementation*.

For normal BTL operation, connect the PBTL pin to local ground.

7.3.7 Short-Circuit Protection and Automatic Recovery Feature

TPA3113D2 has protection from overcurrent conditions caused by a short circuit on the output stage. The short circuit protection fault is reported on the $\overline{\text{FAULT}}$ pin as a low state. The amplifier outputs are switched to a Hi-Z state when the short-circuit protection latch is engaged. The latch can be cleared by cycling the $\overline{\text{SD}}$ pin through the low state.

If automatic recovery from the short-circuit protection latch is desired, connect the $\overline{\text{FAULT}}$ pin directly to the $\overline{\text{SD}}$ pin. This allows the $\overline{\text{FAULT}}$ pin function to automatically drive the $\overline{\text{SD}}$ pin low which clears the short-circuit protection latch.

7.3.8 Thermal Protection

Thermal protection on the TPA3113D2 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15°C tolerance on this trip point from device to device. When the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 15°C. The device begins normal operation at this point with no external system interaction.

Thermal protection faults are NOT reported on the $\overline{\text{FAULT}}$ terminal.

7.4 Device Functional Modes

7.4.1 TPA3113D2 Modulation Scheme

The TPA3113D2 uses a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load. Each output is switching from 0 volts to the supply voltage. The OUTP and OUTN are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTP is greater than 50% and OUTN is less than 50% for positive output voltages. The duty cycle of OUTP is less than 50% and OUTN is greater than 50% for negative output voltages. The voltage across the load sits at 0 V throughout most of the switching period, reducing the switching current, which reduces any I^2R losses in the load.

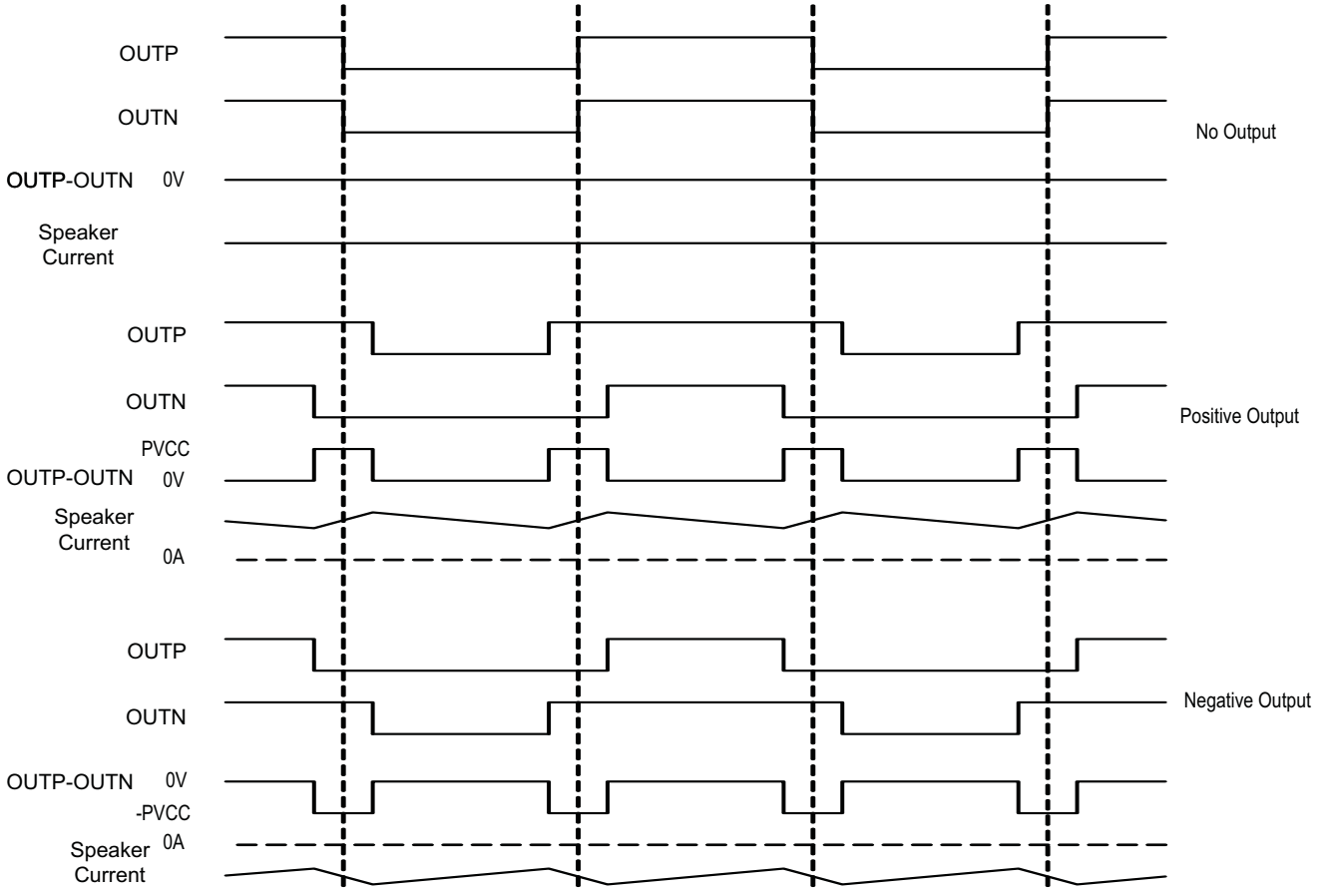


Figure 30. The TPA3113D2 Output Voltage and Current Waveforms Into an Inductive Load

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPA3113D2 is designed for use in stereo speakers like in TV sets, sound docks, and Bluetooth speakers. The TPA3113D2 can either be configured in stereo or mono mode, depending on output power conditions. Depending on output power requirements and necessity for (speaker) load protection, the built-in PLIMIT circuit can be used to control system power.

8.2 Typical Applications

8.2.1 Stereo Class-D Amplifier With BTL Output

Stereo Class-D Amplifier with BTL Output and Differential-Ended Inputs, use ferrite bead and capacitor as the output filter.

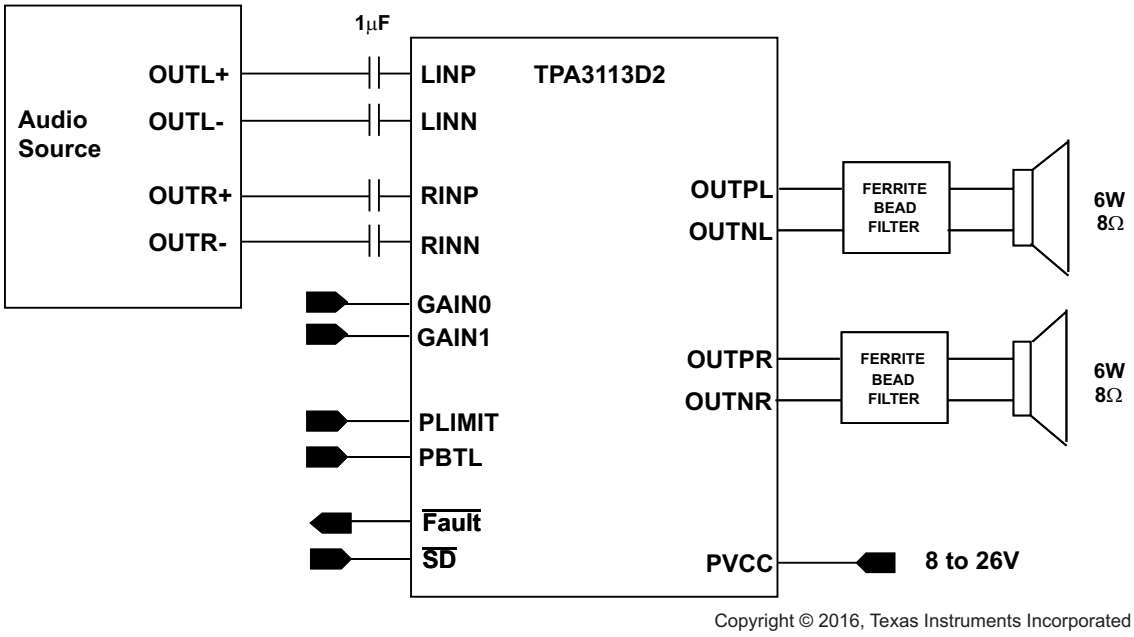


Figure 31. Simplified Application Schematic

8.2.1.1 Design Requirements

Table 4 lists the design parameters for this example.

Table 4. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range PVDD	8 V to 26 V
Ferrite bead + capacitor	120 Ω to 600 Ω at 100 MHz + 1 nF / 2.2 nF

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Ferrite Bead Filter Considerations

Using the Advanced Emissions Suppression Technology in the TPA3113D2 amplifier it is possible to design a high efficiency Class-D audio amplifier while minimizing interference to surrounding circuits. It is also possible to accomplish this with only a low-cost ferrite bead filter. In this case it is necessary to carefully select the ferrite bead used in the filter.

One important aspect of the ferrite bead selection is the type of material used in the ferrite bead. Not all ferrite material is alike, so it is important to select a material that is effective in the 10 to 100 MHz range which is key to the operation of the Class D amplifier. Many of the specifications regulating consumer electronics have emissions limits as low as 30 MHz. It is important to use the ferrite bead filter to block radiation in the 30 MHz and above range from appearing on the speaker wires and the power supply lines which are good antennas for these signals. The impedance of the ferrite bead can be used along with a small capacitor with a value in the range of 1000 pF to reduce the frequency spectrum of the signal to an acceptable level. For best performance, the resonant frequency of the ferrite bead/ capacitor filter should be less than 10 MHz.

Also, it is important that the ferrite bead is large enough to maintain its impedance at the peak currents expected for the amplifier. Some ferrite bead manufacturers specify the bead impedance at a variety of current levels. In this case, it is possible to make sure the ferrite bead maintains an adequate amount of impedance at the peak current of the amplifier. If these specifications are not available, it is also possible to estimate the bead current handling capability by measuring the resonant frequency of the filter output at low power and at maximum power. A change of resonant frequency of less than fifty percent under this condition is desirable. Examples of ferrite beads which have been tested and work well with the TPA3113D2 include 28L0138-80R-10 and HI1812V101R-10 from Steward and the 742792510 from Wurth Electronics.

A high-quality ceramic capacitor is also needed for the ferrite bead filter. A low ESR capacitor with good temperature and voltage characteristics works best.

Additional EMC improvements may be obtained by adding snubber networks from each of the class D outputs to ground. Suggested values for a simple RC series snubber network would be 10 Ω in series with a 330-pF capacitor although design of the snubber network is specific to every application and must be designed considering the parasitic reactance of the printed-circuit board as well as the audio amp. Take care to evaluate the stress on the component in the snubber network especially if the amp is running at high PVCC. Also, make sure the layout of the snubber network is tight and returns directly to the PGND or the PowerPAD™ beneath the chip.

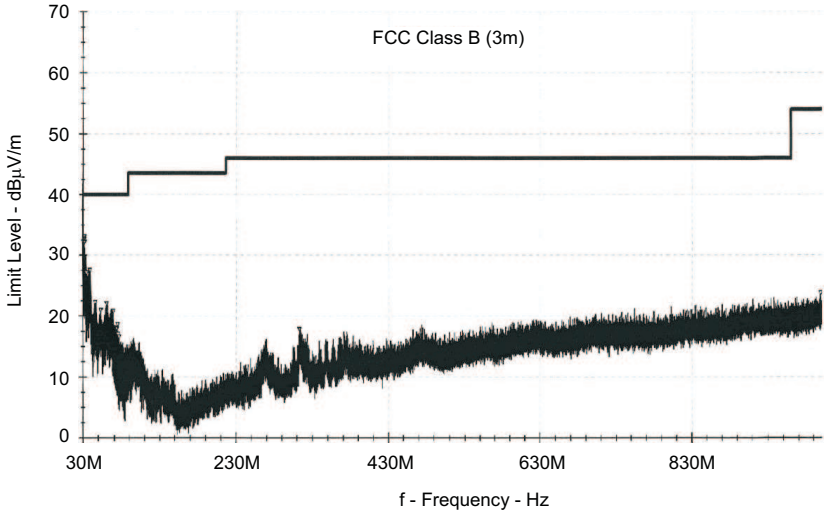


Figure 32. TPA3113D2 EMC Spectrum With FCC Class B Limits

8.2.1.2.2 Efficiency: LC Filter Required With the Traditional Class-D Modulation Scheme

The main reason that the traditional class-D amplifier needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme, because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is 2 × V_{CC}, and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The TPA3113D2 modulation scheme has little loss in the load without a filter because the pulses are short and the change in voltage is V_{CC} instead of 2 × V_{CC}. As the output power increases, the pulses widen, making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance but higher impedance at the switching frequency than the speaker, which results in less power dissipation, therefore increasing efficiency.

8.2.1.2.3 When to Use an Output Filter for EMI Suppression

The TPA3113D2 has been tested with a simple ferrite bead filter for a variety of applications including long speaker wires up to 125 cm and high power. The TPA3113D2 EVM passes FCC Class B specifications under these conditions using twisted speaker wires. The size and type of ferrite bead can be selected to meet application requirements. Also, the filter capacitor can be increased if necessary with some impact on efficiency.

There may be a few circuit instances where it is necessary to add a complete LC reconstruction filter. These circumstances might occur if there are nearby circuits which are sensitive to noise. In these cases, a classic second order Butterworth filter similar to those shown in the figures below can be used.

Some systems have little power supply decoupling from the AC line but are also subject to line conducted interference (LCI) regulations. These include systems powered by *wall warts* and *power bricks*. In these cases, it LC reconstruction filters can be the lowest cost means to pass LCI tests. Common-mode chokes using low frequency ferrite material can also be effective at preventing line conducted interference.

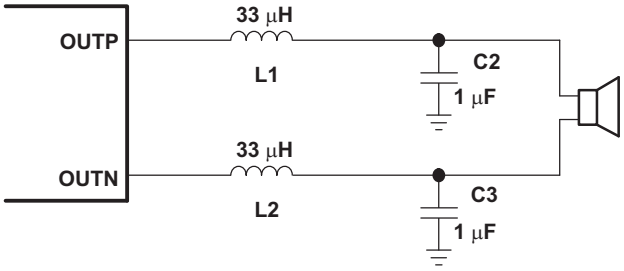


Figure 33. Typical LC Output Filter, Cutoff Frequency of 27 kHz, Speaker Impedance = 8 Ω

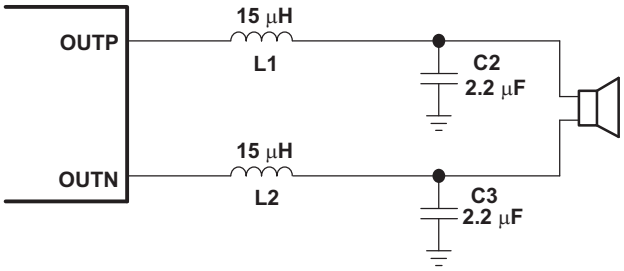


Figure 34. Typical LC Output Filter, Cutoff Frequency of 27 kHz, Speaker Impedance = 4 Ω

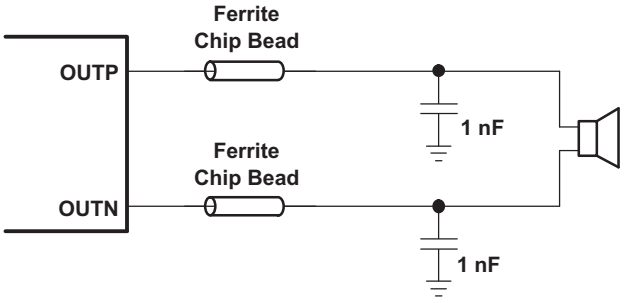
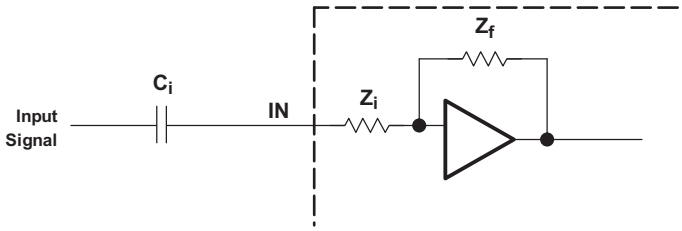


Figure 35. Typical Ferrite Chip Bead Filter (Chip Bead Example)

8.2.1.2.4 Input Resistance

Changing the gain setting can vary the input resistance of the amplifier from its smallest value, 9 kΩ ±20%, to the largest value, 60 kΩ ±20%. As a result, if a single capacitor is used in the input high-pass filter, the –3 dB or cutoff frequency may change when changing gain steps.



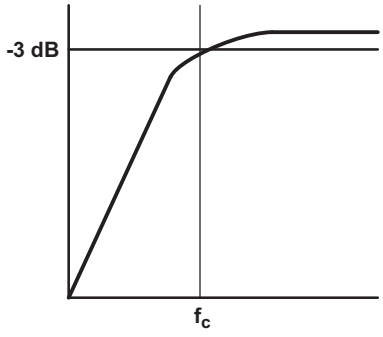
The –3-dB frequency can be calculated using Equation 2. Use the Z_I values given in Table 1.

$$f = \frac{1}{2\pi Z_i C_i} \tag{2}$$

8.2.1.2.5 Input Capacitor, C_I

In the typical application, an input capacitor C_I) is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C_I and the input impedance of the amplifier (Z_I) form a high-pass filter with the corner frequency determined in Equation 3.

$$\mathbf{f_c = \frac{1}{2\pi Z_i C_i}} \tag{3}$$



The value of C_I is important, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where Z_I is 60 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 3 is reconfigured as Equation 4.

$$C_i = \frac{1}{2\pi Z_i f_c} \tag{4}$$

In this example, C_I is 0.13 µF; so, one would likely choose a value of 0.15 µF as this value is commonly used. If the gain is known and is constant, use Z_I from Table 1 to calculate C_I. A further consideration for this capacitor is the leakage path from the input source through the input network C_I) and the feedback network to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at 3 V, which is likely higher than the source DC level. Note that it is important to confirm the capacitor polarity in the application. Additionally, lead-free solder can create DC offset voltages and it is important to ensure that boards are cleaned properly.

8.2.1.2.6 BSN and BSP Capacitors

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 0.22-µF ceramic capacitor, rated for at least 25 V, must be connected from each output to its corresponding bootstrap input. Specifically, one 0.22-µF capacitor must be connected from OUTPx to BSPx, and one 0.22-µF capacitor must be connected from OUTNx to BSNx (see the application circuit diagram in Figure 31).

The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

8.2.1.2.7 Differential Inputs

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the TPA3113D2 with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the TPA3113D2 with a single-ended source, AC ground the INP or INN input through a capacitor equal in value to the input capacitor on INN or INP and apply the audio source to either input. In a single-ended input application, the unused input should be ac grounded at the audio source instead of at the device input for best noise performance. For good transient performance, the impedance seen at each of the two differential inputs must be the same.

The impedance seen at the inputs must be limited to an RC time constant of 1 ms or less if possible. This is to allow the input DC blocking capacitors to become completely charged during the 14-ms power-up time. If the input capacitors are not allowed to completely charge, there is some additional sensitivity to component matching which can result in pop if the input components are not well matched.

8.2.1.2.8 Using LOW-ESR Capacitors

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

8.2.1.3 Application Curves

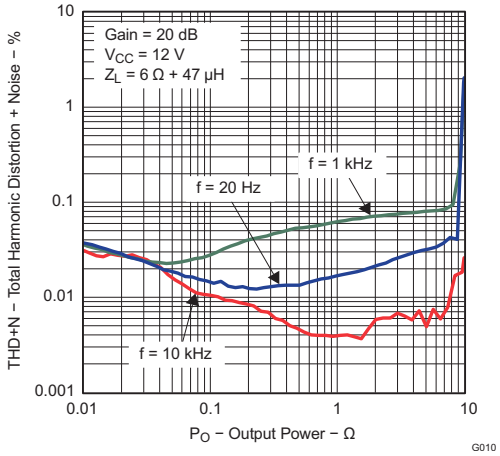


Figure 36. Total Harmonic Distortion + Noise vs Output Power (BTL)

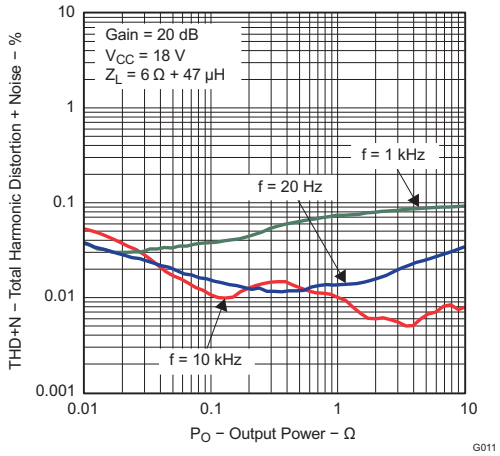


Figure 37. Total Harmonic Distortion + Noise vs Output Power (BTL)

8.2.2 Stereo Class-D Amplifier With BTL Output

TPA3113D2 is a very flexible and easy to use Class D amplifier; Therefore the design process is straightforward. Before beginning the design, gather the following information regarding the audio system.

- PVCC rail planned for the design
- Speaker or load impedance
- Maximum output power requirement
- Output filter design

For example, Select PVCC = 12 V, speaker load = 4 Ω, Maximum output power is 6 W, the peak output current is 1.73 A, and make sure the rate current of ferrite bead has enough margin. Generally, select ferrite bead with larger impedance will get a better EMI result. Some application case need pass the conducted emissions test with some poor EMI filter in the power supply system, in this case, suggest to add an EMI filter on PVCC. Take application note *AN-2162 Simple Success With Conducted EMI From DC-DC Converters* as the reference.

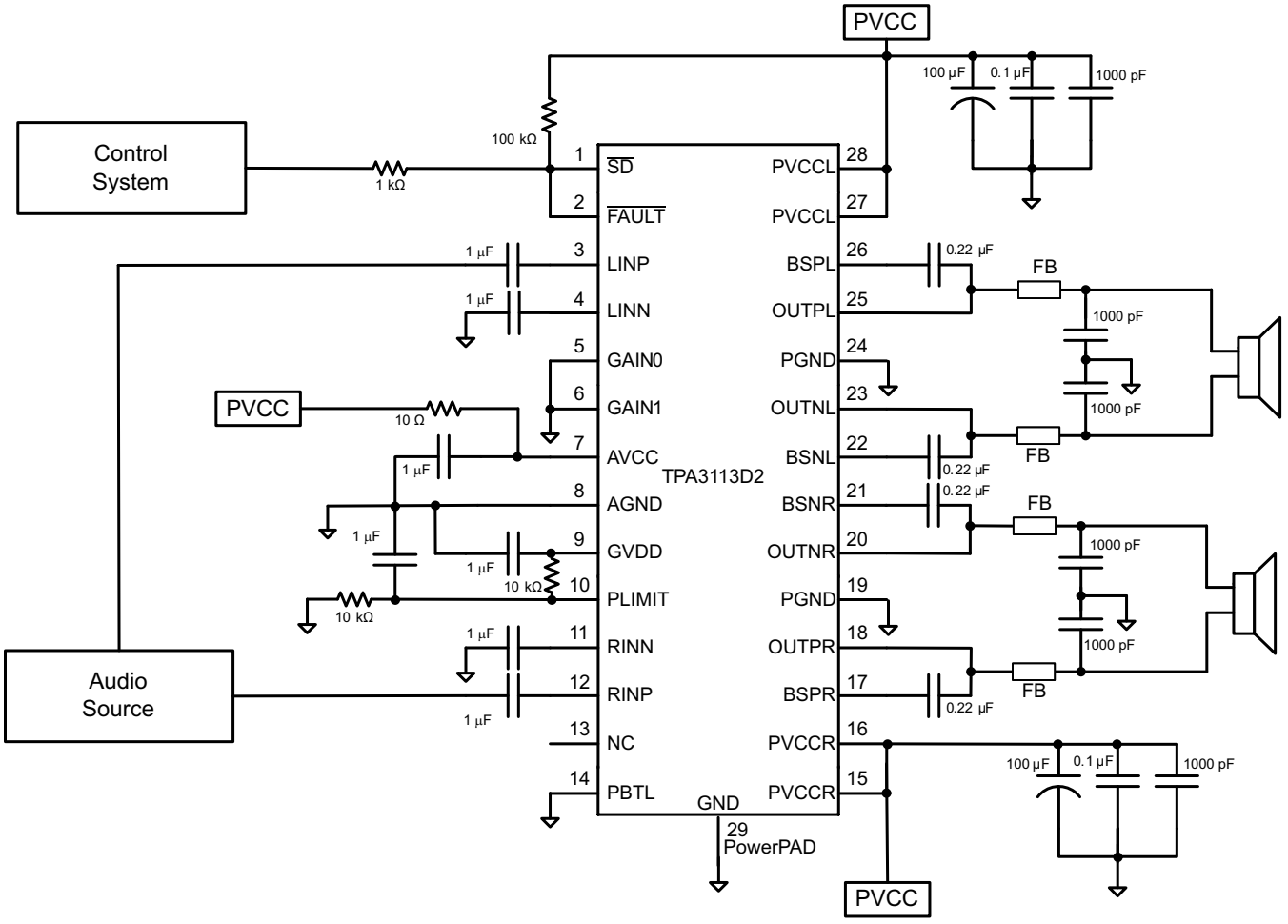


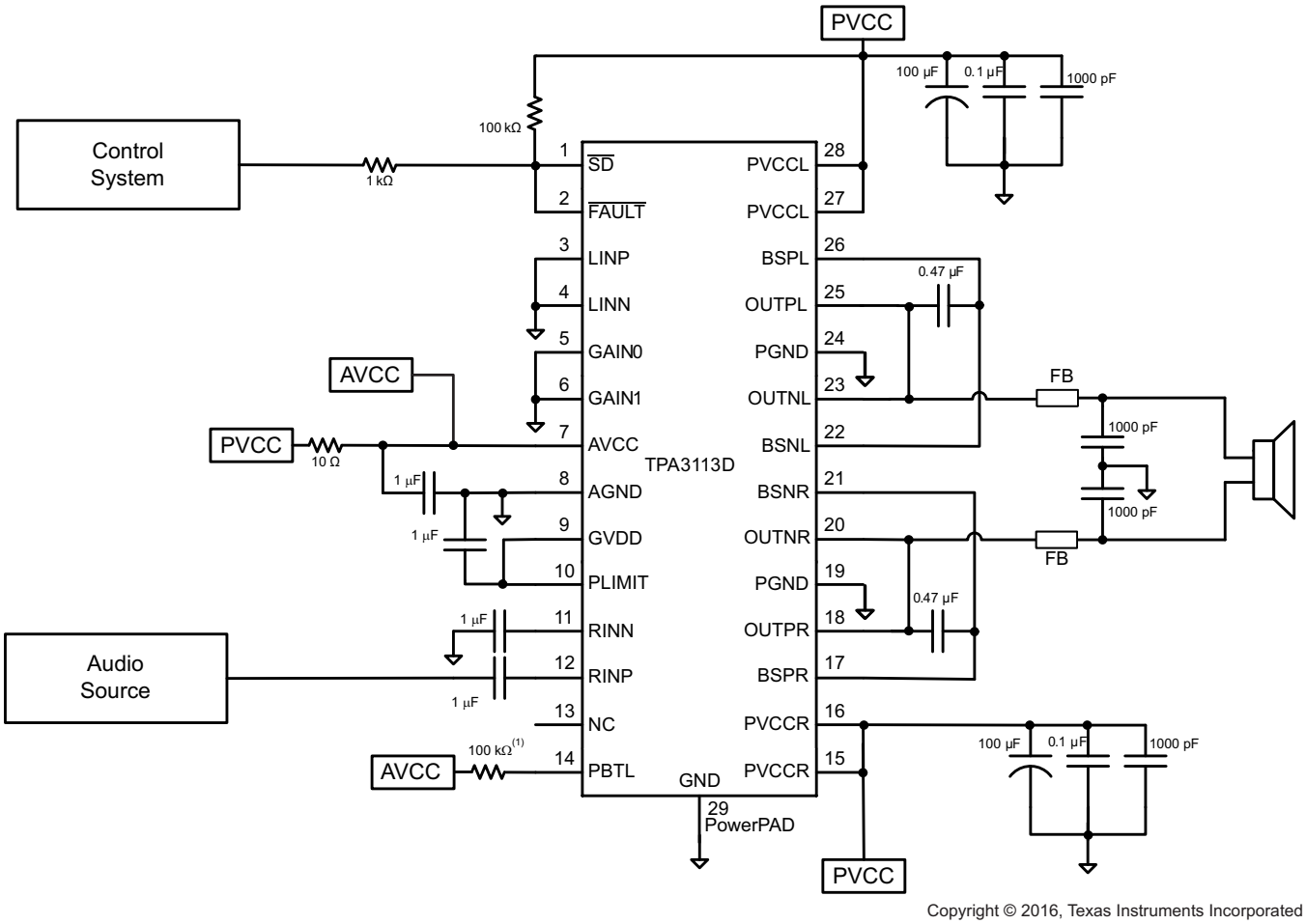
Figure 38. Stereo Class-D Amplifier With BTL Output and Single-Ended Inputs With Power Limiting

8.2.3 Stereo Class-D Amplifier With PBTL Output

TPA3113D2 also support MONO mode. Before beginning the design, gather the following information regarding the audio system.

- PVCC rail planned for the design
- Speaker or load impedance
- Maximum output power requirement
- Output filter design

For example, Select PVCC = 18 V, speaker load = 4 Ω, Maximum output power is 8 W, the peak output current is 2 A, and make sure ferrite bead's rate current has enough margin. Generally, select ferrite bead with larger impedance will get a better EMI result. Some application case need pass the conducted emissions test with some poor EMI filter in the power supply system, in this case, suggest to add an EMI filter on PVCC. Take application note *AN-2162 Simple Success With Conducted EMI From DC-DC Converters* as the reference.



(1) 100-kΩ resistor is needed if the PVCC slew rate is more than 10 V/ms.

Figure 39. Stereo Class-D Amplifier With PBTL Output and Single-Ended Input

9 Power Supply Recommendations

9.1 Power Supply Decoupling, C_S

The TPA3113D2 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. Optimum decoupling is achieved by using a network of capacitors of different types that target specific types of noise on the power supply leads. For higher frequency transients due to parasitic circuit elements such as bond wire and copper trace inductances as well as lead frame capacitance, a good-quality low equivalent-series-resistance (ESR) ceramic capacitor of value between 220 pF and 1000 pF works well. This capacitor must be placed as close to the device PVCC pins and system ground (either PGND pins or PowerPAD) as possible. For mid-frequency noise due to filter resonances or PWM switching transients as well as digital hash on the line, another good-quality capacitor typically 0.1 μF to 1 μF placed as close as possible to the device PVCC leads works best. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 220 μF or greater placed near the audio power amplifier is recommended. The 220-μF capacitor also serves as a local storage capacitor for supplying current during large signal transients on the amplifier outputs. The PVCC terminals provide the power to the output transistors, so a 220-μF or larger capacitor should be placed on each PVCC terminal. A 10-μF capacitor on the AVCC terminal is adequate. Also, a small decoupling resistor between AVCC and PVCC can be used to keep high frequency class D noise from entering the linear input amplifiers.

10 Layout

10.1 Layout Guidelines

The TPA3113D2 can be used with a small, inexpensive ferrite bead output filter for most applications. However, because the Class-D switching edges are fast, it is necessary to take care when planning the layout of the printed-circuit board. The following suggestions help to meet EMC requirements.

- Decoupling capacitors—The high-frequency decoupling capacitors must be placed as close to the PVCC and AVCC terminals as possible. Large (220 μF or greater) bulk power supply decoupling capacitors should be placed near the TPA3113D2 on the PVCCL and PVCCR supplies. Local, high-frequency bypass capacitors must be placed as close to the PVCC pins as possible. These capacitors can be connected to the thermal pad directly for an excellent ground connection. Consider adding a small, good-quality low ESR ceramic capacitor between 220 pF and 1000 pF and a larger mid-frequency cap of value between 0.1 μF and 1 μF also of good quality to the PVCC connections at each end of the chip.
- Keep the current loop from each of the outputs through the ferrite bead and the small filter cap and back to PGND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.
- Grounding—The AVCC (pin 7) decoupling capacitor must be grounded to analog ground (AGND). The PVCC decoupling capacitors should connect to PGND. Analog ground and power ground should be connected at the thermal pad, which must be used as a central ground connection or star ground for the TPA3113D2.
- Output filter—The ferrite EMI filter (Figure 35) must be placed as close to the output terminals as possible for the best EMI performance. The LC filter (Figure 33 and Figure 34) must be placed close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded to power ground.
- Thermal Pad—The thermal pad must be soldered to the PCB for proper thermal performance and optimal reliability. The dimensions of the thermal pad and thermal land should be 6.46 mm by 2.35 mm. Seven rows of solid vias (three vias per row, 0,3302 mm or 13 mils diameter) must be equally spaced underneath the thermal land. The vias must connect to a solid copper plane, either on an internal layer or on the bottom layer of the PCB. The vias must be solid vias, not thermal relief or webbed vias. See the TI Application Report *Quad Flatpack No-Lead Logic Packages* for more information about using the TSSOP thermal pad. For recommended PCB footprints, see figures at the end of this data sheet.

For an example layout, see the *TPA3113D2 EVM Audio Amplifier Evaluation Board*. Both the EVM user manual and the thermal pad application report are available on the TI Web site at http://www.ti.com.

Layout Guidelines (continued)

10.1.1 PCB Material Recommendation

TI recommends using FR-4 Glass Epoxy material with 1 oz. (35 μm) for the TPA3113D2. The use of this material can provide for higher power output, improved thermal performance, and better EMI margin (due to lower PCB trace inductance). TI recommends using several GND underneath the device thermal pad for thermal coupling to a bottom side copper GND plane for best thermal performance.

10.2 Layout Example

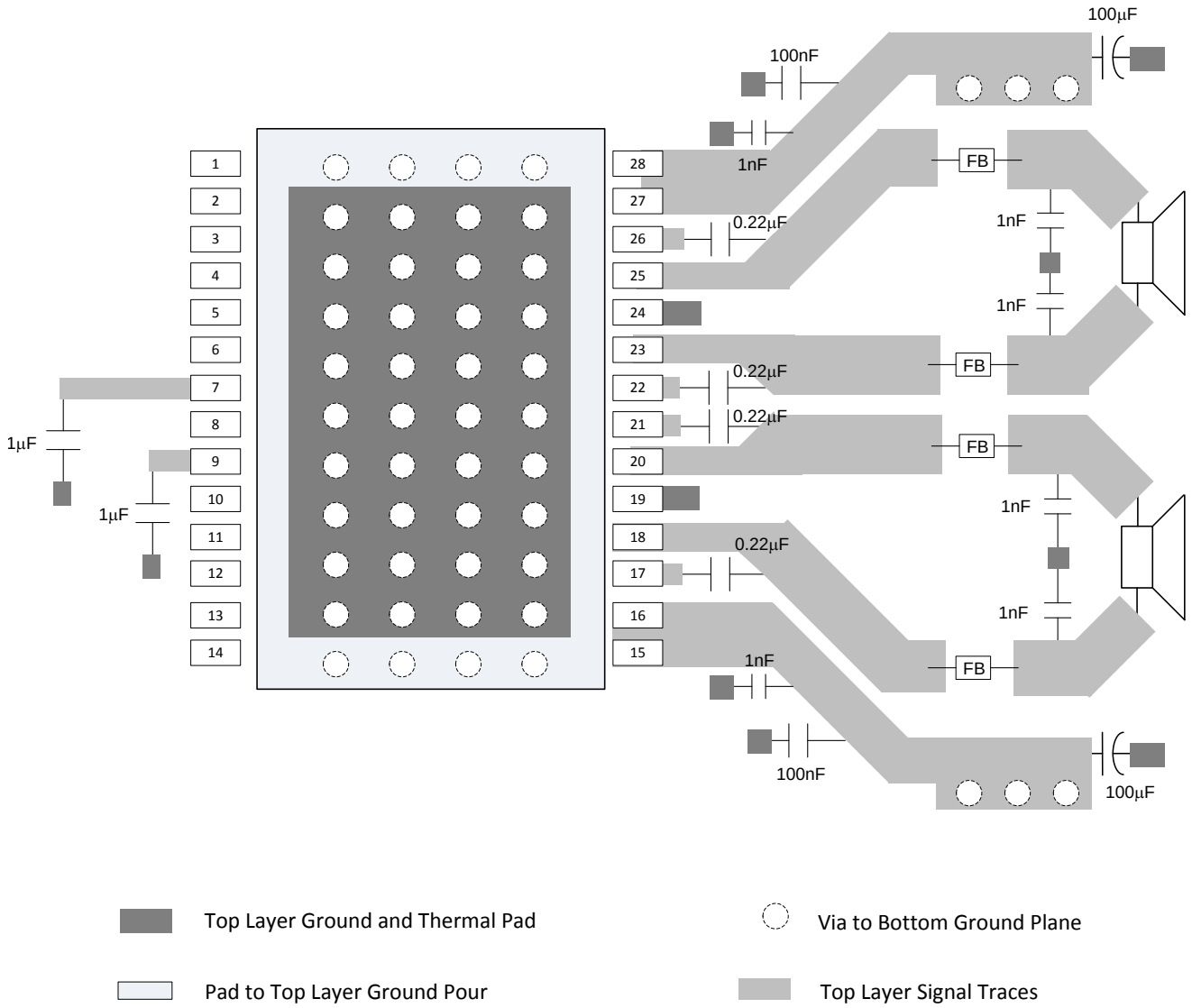


Figure 40. BTL Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- *AN-2162 Simple Success With Conducted EMI From DC-DC Converters* (SNVA489)
- *Quad Flatpack No-Lead Logic Packages* (SCBA017)
- *TPA3113D2 EVM Audio Amplifier Evaluation Board* (SLOUS271)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

SpeakerGuard, PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPA3113D2PWP	Active	Production	HTSSOP (PWP) | 28	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3113D2
TPA3113D2PWP.A	Active	Production	HTSSOP (PWP) | 28	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3113D2
TPA3113D2PWP.B	Active	Production	HTSSOP (PWP) | 28	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3113D2
TPA3113D2PWPR	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3113D2
TPA3113D2PWPR.A	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3113D2
TPA3113D2PWPR.B	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3113D2
TPA3113D2PWPRG4	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3113D2
TPA3113D2PWPRG4.A	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3113D2
TPA3113D2PWPRG4.B	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3113D2

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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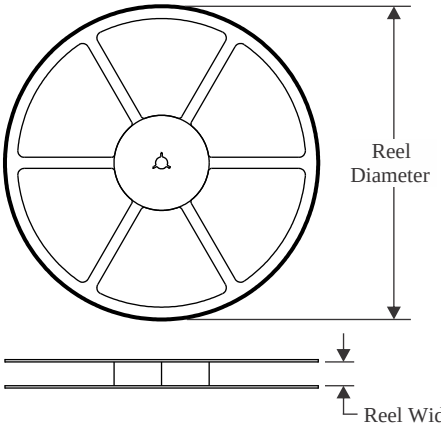
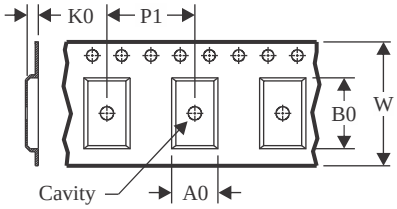
TAPE AND REEL INFORMATION

REEL DIMENSIONS

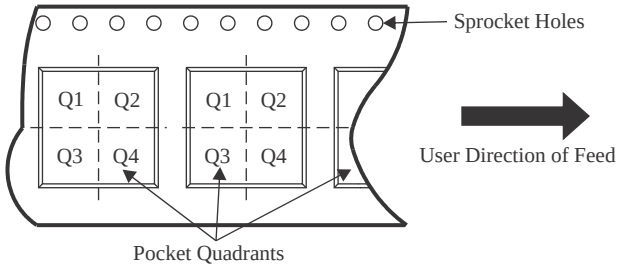


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

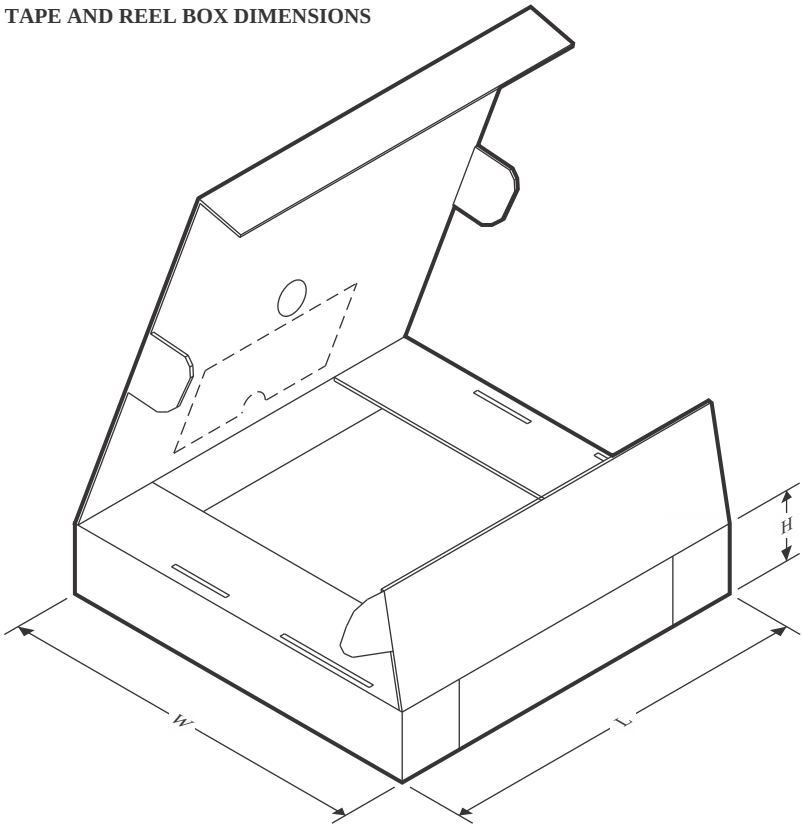
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA3113D2PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TPA3113D2PWPRG4	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

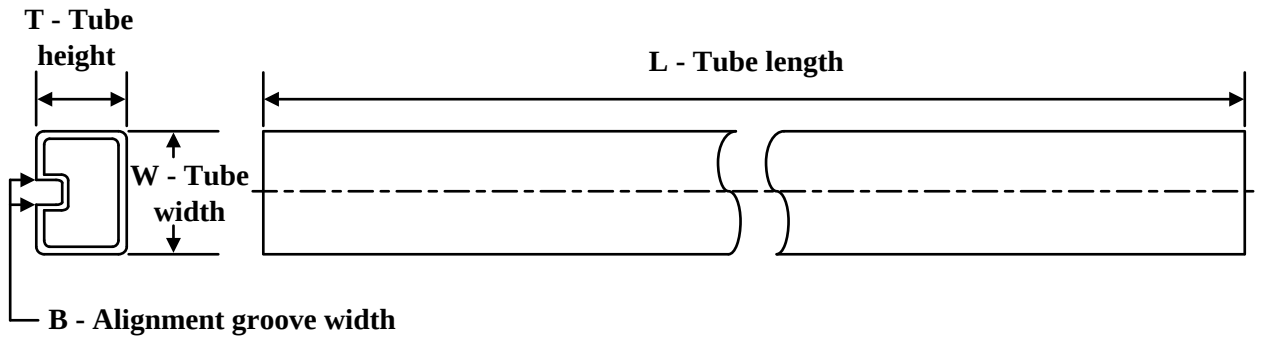
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA3113D2PWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0
TPA3113D2PWPRG4	HTSSOP	PWP	28	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPA3113D2PWP	PWP	HTSSOP	28	50	530	10.2	3600	3.5
TPA3113D2PWP.A	PWP	HTSSOP	28	50	530	10.2	3600	3.5
TPA3113D2PWP.B	PWP	HTSSOP	28	50	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

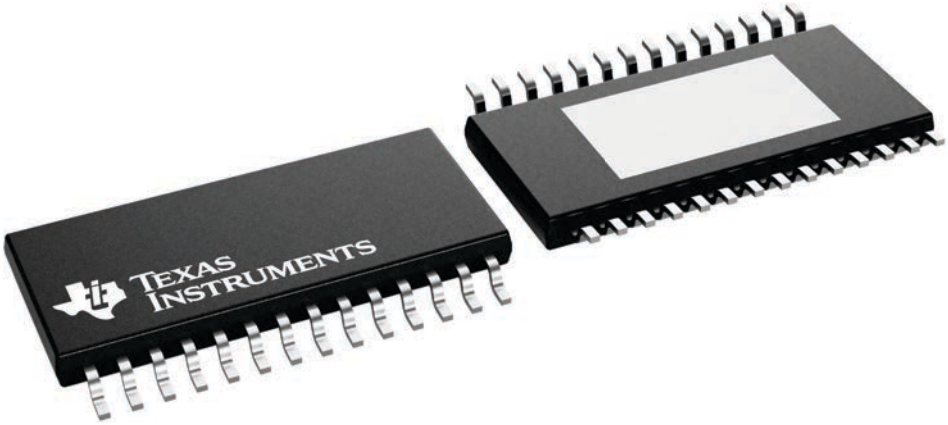
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

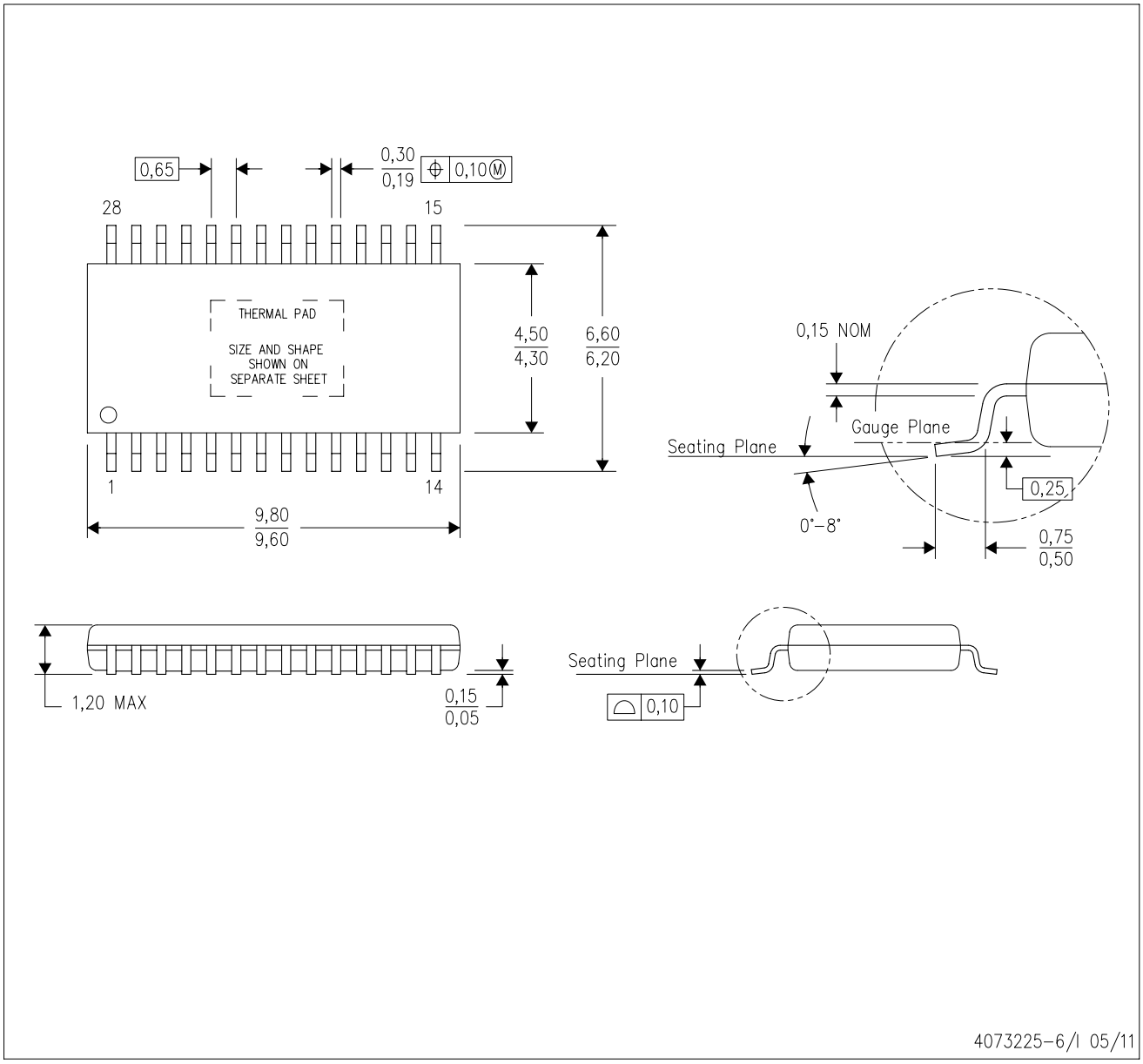
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

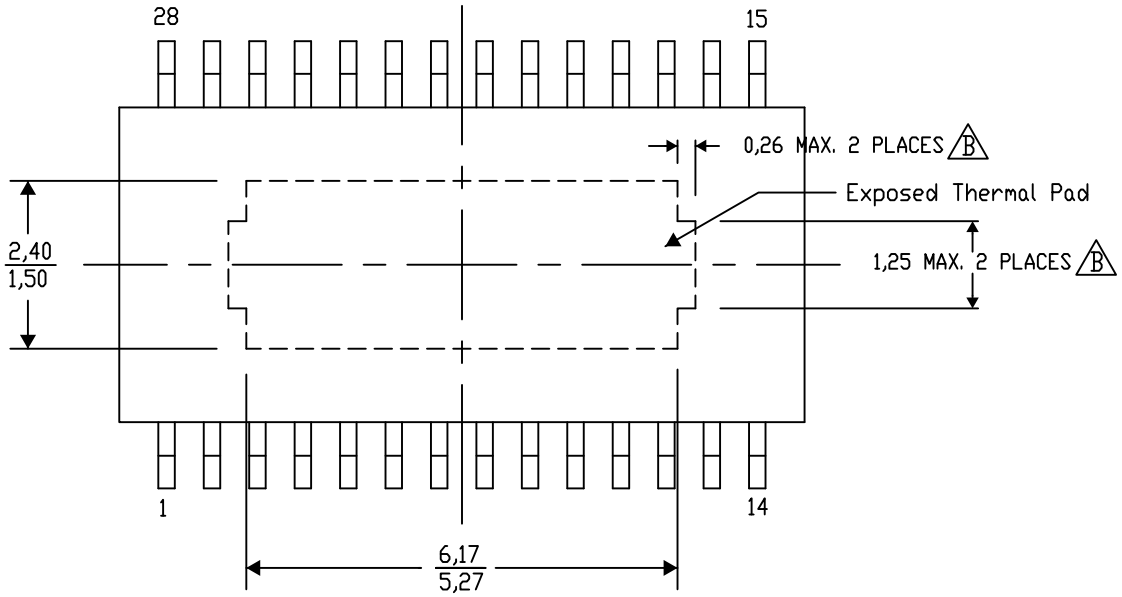
PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

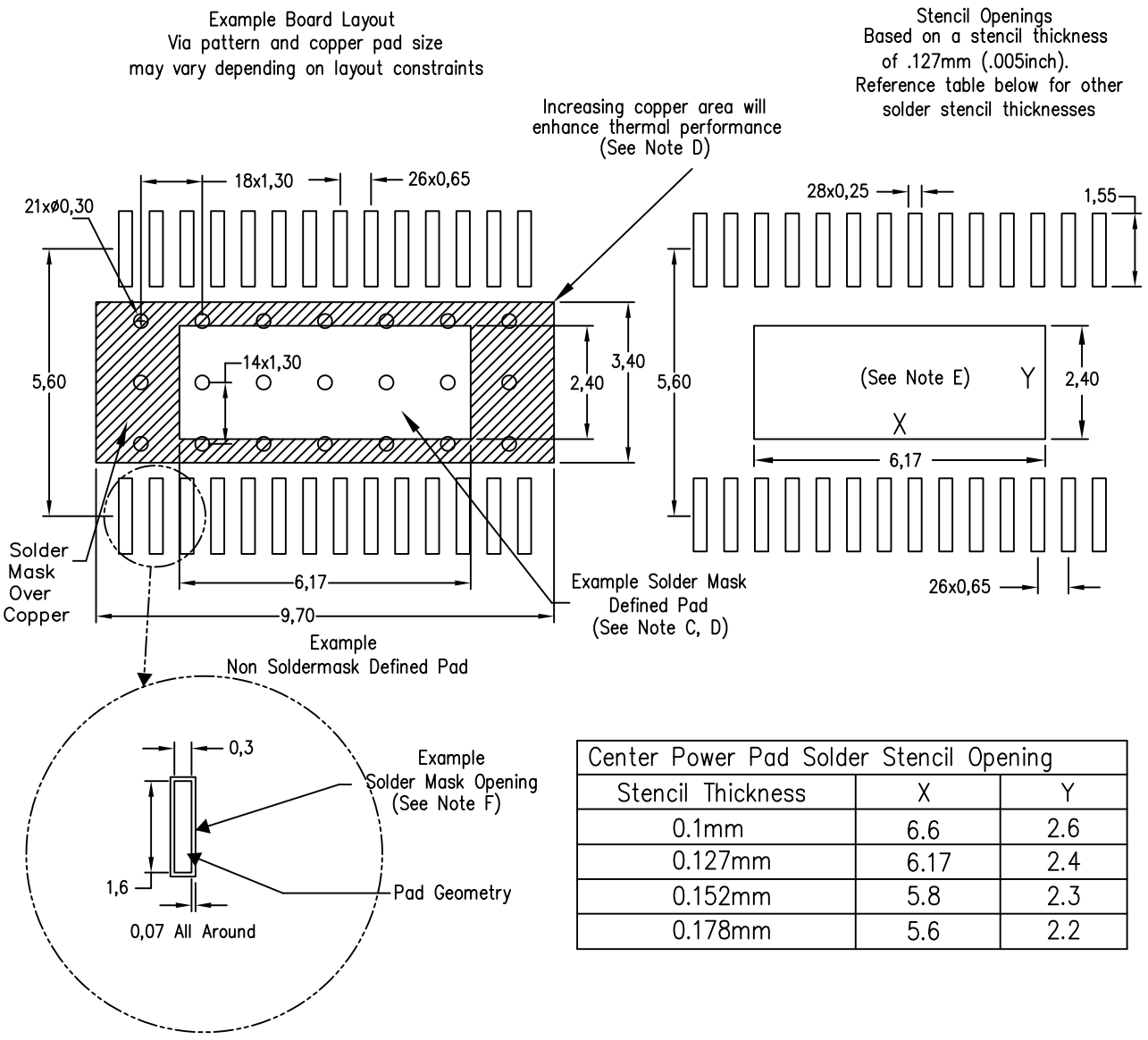
4206332–33/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.6	2.6
0.127mm	6.17	2.4
0.152mm	5.8	2.3
0.178mm	5.6	2.2

4207609–19/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
E. For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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