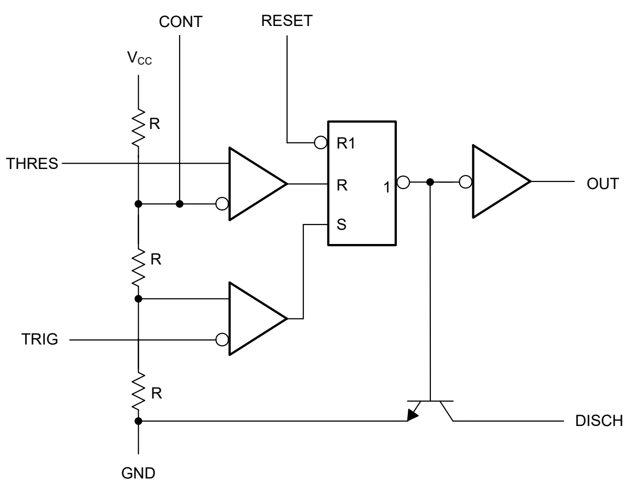
# Nx556, Sx556 Dual Precision Timers

## 1 Features

- Two precision timing circuits per package
- Astable or monostable operation
- TTL-compatible output can sink or source up to 200mA
- Active pullup or pulldown

## 2 Applications

- Precision timers from microseconds to hours
- Pulse-shaping circuits
- Missing-pulse detectors
- Pulse-width modulators
- Pulse-position modulators
- Sequential timers
- Pulse generators
- Frequency dividers
- Application timers
- Industrial controls




**Simplified Schematic (Each Timer)**

## 3 Description

The Nx556 and Sx556 devices provide two independent timing circuits of the NA555, NE555, SA555, or SE555 type in each package. These circuits operate in an astable or monostable mode with external resistor-capacitor (RC) timing control. The basic timing provided by the RC time constant is controlled actively by modulating the bias of the control-voltage input.

Each timer has a trigger level equal to approximately one-third of the supply voltage and a threshold level equal to approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage pin (CONT). When the trigger input (TRIG) is less than the trigger level, the flip-flop is set and the output goes high. If TRIG is greater than the trigger level and the threshold input (THRES) is greater than the threshold level, the flip-flop is reset and the output is low. The reset input (RESET) overrides all other inputs and is used to initiate a new timing cycle. If RESET is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge pin (DISCH) and the ground pin (GND). Tie all unused inputs to an appropriate logic level to prevent false triggering.

**Device Information**

| PART NUMBER | OPERATING TEMPERATURE | PACKAGE[(1)] |
|---|---|---|
| NA556 | $T_A$ = –40°C to +105°C | D (SOIC, 14) |
| | | N (PDIP, 14) |
| NE556 | $T_A$ = 0°C to 70°C | D (SOIC, 14) |
| | | DB (SSOP, 14) |
| | | N (PDIP, 14) |
| | | NS (SO, 14) |
| SA556 | $T_A$ = –40°C to +85°C | N (PDIP, 14) |
| SE556 | $T_A$ = –55°C to +125°C | J (CDIP, 14) |

(1) For more information, see Section 10.

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## 4 Pin Configuration and Functions

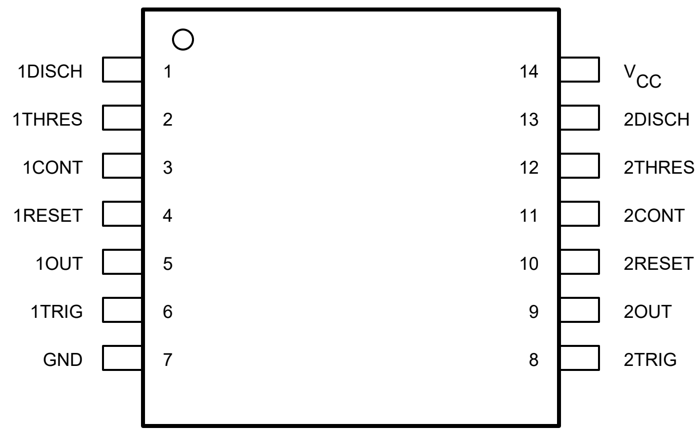



**Figure 4-1. NA556: D, 14-Pin SOIC, and N, 14-Pin PDIP**
**NE556: D, 14-Pin SOIC, DB, 14-Pin SSOP, N, 14-Pin PDIP, and NS, 14-Pin SO**
**SA556: N, 14-Pin PDIP**
**SE556: J, 14-Pin CDIP**
**(Top View)**

**Table 4-1. Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| CONT | 3, 11 | Input | Controls comparator thresholds. Outputs 2/3 $V_{CC}$ and allows bypass capacitor connection. |
| DISCH | 1, 13 | Output | Open collector output to discharge timing capacitor. |
| GND | 7 | — | Ground. |
| OUT | 5, 9 | Output | High current timer output signal. |
| RESET | 4, 10 | Input | Active low reset input forces output and discharge low. |
| THRES | 2, 12 | Input | End of timing input. THRES > CONT sets output low and discharge low. |
| TRIG | 6, 8 | Input | Start of timing input. TRIG < 1/2 CONT sets output high and discharge open. |
| $V_{CC}$ | 14 | — | Power-supply voltage. |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage[(2)] | | | 18 | V |
| $V_I$ | Input voltage: CONT, RESET, THRES, and TRIG | | | $V_{CC}$ | V |
| $I_O$ | Output current | | | ±225 | mA |
| $T_J$ | Operating virtual junction temperature | | | 150 | °C |
| | Lead temperature 1.6mm (1/16 inch) from case | J package, 60 seconds | | 300 | °C |
| | | D, N, or NS package, 10 seconds | | 260 | |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)] | ±500 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002[(2)] | ±1500 | |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | NA556, NE556, SA556 | 4.5 | 16 | V |
| | | SE556 | 4.5 | 18 | |
| $I_O$ | Output current | | | ±200 | mA |
| $T_A$ | Operating free-air temperature | NA556 | –40 | 105 | °C |
| | | NE556 | 0 | 70 | |
| | | SA556 | –40 | 85 | |
| | | SE556 | –55 | 125 | |

## 5.4 Thermal Information

| THERMAL METRIC[(1)] | | NA556, NE556 | NE556 | SE556 | NA556, NE556, SA556 | NE556 | UNIT |
|---|---|---|---|---|---|---|---|
| | | D (SOIC) | DB (SSOP) | J (CDIP) | N (PDIP) | NS (SOP) | |
| | | 14 PINS | 14 PINS | 14 PINS | 14 PINS | 14 PINS | |
| $R_{θJA}$ | Junction-to-ambient thermal resistance | 91.4 | 104.5 | 86.1 | 73.4 | 89.5 | °C/W |
| $R_{θJC(top)}$ | Junction-to-case (top) thermal resistance | 51.7 | 56.3 | 38.8 | 51.7 | 47.3 | °C/W |
| $R_{θJB}$ | Junction-to-board thermal resistance | 49.6 | 64.1 | 73.5 | 47.6 | 52.9 | °C/W |
| $ψ_{JT}$ | Junction-to-top characterization parameter | 12.3 | 14.0 | 32.4 | 29.5 | 11.3 | °C/W |
| $ψ_{JB}$ | Junction-to-board characterization parameter | 49.1 | 63.3 | 68.7 | 47.0 | 52.3 | °C/W |
| $R_{θJC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | 20.1 | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

## 5.5 Electrical Characteristics

at $V_{CC}$ = 5V to 15V and $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_T$ | Threshold voltage level | $V_{CC}$ = 15V | NA556, NE556, SA556 | 8.8 | 10 | 11.2 | V |
| | | | SE556 | 9.4 | 10 | 10.6 | |
| | | $V_{CC}$ = 5V | NA556, NE556, SA556 | 2.4 | 3.3 | 4.2 | |
| | | | SE556 | 2.7 | 3.3 | 4 | |
| $I_T$ | Threshold current[(1)] | | | | 30 | 250 | nA |
| $V_{TRIG}$ | Trigger voltage level | $V_{CC}$ = 15V | NA556, NE556, SA556 | 4.5 | 5 | 5.6 | V |
| | | | SE556 | 4.8 | 5 | 5.2 | |
| | | $V_{CC}$ = 15V, $T_A$ = –55°C to +125°C | SE556 | 3 | | 6 | |
| | | $V_{CC}$ = 5V | NA556, NE556, SA556 | 1.1 | 1.67 | 2.2 | |
| | | | SE556 | 1.45 | 1.67 | 1.9 | |
| | | $V_{CC}$ = 5V, $T_A$ = –55°C to +125°C | SE556 | | | 1.9 | |
| $I_{TRIG}$ | Trigger current | $V_{TRIG}$ = 0V | NA556, NE556, SA556 | | 0.5 | 2 | µA |
| | | | SE556 | | 0.5 | 0.9 | |
| $V_{RESET}$ | Reset voltage level | | | 0.3 | 0.7 | 1 | V |
| | | $T_A$ = –55°C to +125°C | SE556 | | | 1.1 | |
| $I_{RESET}$ | Reset current | $V_{RESET}$ = $V_{CC}$ | | | 0.1 | 0.4 | mA |
| | | $V_{RESET}$ = 0V | NA556, NE556, SA556 | | –0.4 | 1.5 | |
| | | | SE556 | | –0.4 | –1 | |
| $I_{DISCH}$ | Discharge switch off-state current | | | | 20 | 100 | nA |
| $V_{CONT}$ | Control voltage (open circuit) | $V_{CC}$ = 15V | NA556, NE556, SA556 | 9 | 10 | 11 | V |
| | | | SE556 | 9.6 | 10 | 10.4 | |
| | | $V_{CC}$ = 15V, $T_A$ = –55°C to +125°C | SE556 | 9.6 | | 10.4 | |
| | | $V_{CC}$ = 5V | NA556, NE556, SA556 | 2.6 | 3.3 | 4 | |
| | | | SE556 | 2.9 | 3.3 | 3.8 | |
| | | $V_{CC}$ = 5V, $T_A$ = –55°C to +125°C | SE556 | 2.9 | | 3.8 | |

## 5.5 Electrical Characteristics (continued)

at $V_{CC}$ = 5V to 15V and $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = 15V, $I_{OL}$ = 10mA | NA556, NE556, SA556 | | 0.1 | 0.25 | V |
| | | | SE556 | | 0.1 | 0.15 | |
| | | $V_{CC}$ = 15V, $I_{OL}$ = 10mA, $T_A$ = –55°C to +125°C | SE556 | | | 0.2 | |
| | | $V_{CC}$ = 15V, $I_{OL}$ = 50mA | NA556, NE556, SA556 | | 0.4 | 0.75 | |
| | | | SE556 | | 0.4 | 0.5 | |
| | | $V_{CC}$ = 15V, $I_{OL}$ = 50mA, $T_A$ = –55°C to +125°C | SE556 | | | 1 | |
| | | $V_{CC}$ = 15V, $I_{OL}$ = 100mA | NA556, NE556, SA556 | | 2 | 2.5 | |
| | | | SE556 | | 2 | 2.2 | |
| | | $V_{CC}$ = 15V, $I_{OL}$ = 100mA, $T_A$ = –55°C to +125°C | SE556 | | | 2.7 | |
| | | $V_{CC}$ = 15V, $I_{OL}$ = 200mA | | | 2.5 | | |
| | | $V_{CC}$ = 5V, $I_{OL}$ = 3.5mA, $T_A$ = –55°C to +125°C | SE556 | | | 0.35 | |
| | | $V_{CC}$ = 5V, $I_{OL}$ = 5mA | NA556, NE556, SA556 | | 0.1 | 0.25 | |
| | | | SE556 | | 0.1 | 0.15 | |
| | | $V_{CC}$ = 5V, $I_{OL}$ = 5mA, $T_A$ = –55°C to +125°C | SE556 | | | 0.8 | |
| | | $V_{CC}$ = 5V, $I_{OL}$ = 8mA | NA556, NE556, SA556 | | 0.15 | 0.3 | |
| | | | SE556 | | 0.15 | 0.25 | |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = 15V, $I_{OH}$ = –100mA | NA556, NE556, SA556 | 12.75 | 13.3 | | V |
| | | | SE556 | 13 | 13.3 | | |
| | | $V_{CC}$ = 15V, $I_{OH}$ = –100mA, $T_A$ = –55°C to +125°C | SE555 | 12 | | | |
| | | $V_{CC}$ = 15V, $I_{OH}$ = –200mA | | | 12.5 | | |
| | | $V_{CC}$ = 5V, $I_{OH}$ = –100mA | NA556, NE556, SA556 | 2.75 | 3.3 | | |
| | | | SE556 | 3 | 3.3 | | |
| | | $V_{CC}$ = 5V, $I_{OH}$ = –100mA, $T_A$ = –55°C to +125°C | SE555 | 2 | | | |

## 5.5 Electrical Characteristics (continued)

at $V_{CC}$ = 5V to 15V and $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Supply current | Output low, no load, $V_{CC}$ = 15V | NA556, NE556, SA556 | | 20 | 30 | mA |
| | | | SE556 | | 20 | 24 | |
| | | Output low, no load, $V_{CC}$ = 5V | NA556, NE556, SA556 | | 6 | 12 | |
| | | | SE556 | | 6 | 10 | |
| | | Output high, no load, $V_{CC}$ = 15V | NA556, NE556, SA556 | | 18 | 26 | |
| | | | SE556 | | 18 | 20 | |
| | | Output high, no load, $V_{CC}$ = 5V | NA556, NE556, SA556 | | 4 | 10 | |
| | | | SE556 | | 4 | 8 | |

(1) This parameter influences the maximum value of the timing resistors $R_A$ and $R_B$ in the circuit of Figure 6-3. For example, when $V_{CC}$ = 5V, the maximum value is $R_A + R_B \cong 3.4M\Omega$, and for $V_{CC}$ = 15V, the maximum value is $R_A + R_B \cong 10M\Omega$.

## 5.6 Switching Characteristics

$V_{CC}$ = 5V and 15V, $T_A$ = 25°C (unless otherwise noted); characteristic values are specified by design, characterization, or both, and are not production tested

| PARAMETER | | TEST CONDITIONS(1) | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| | Temperature coefficient of timing interval | Each timer, monostable(2), $T_A$ = MIN to MAX | NA556, NE556, SA556 | | 50 | | ppm/°C |
| | | | SE556 | | 30 | 100 | |
| | | Each timer, astable(3), $T_A$ = MIN to MAX | NA556, NE556, SA556 | | 150 | | |
| | | | SE556 | | 90 | | |
| | | Timer 1 – Timer 2, $T_A$ = MIN to MAX | | | ±10 | | |
| | Supply voltage sensitivity of timing interval | Each timer, monostable(2) | NA556, NE556, SA556 | | 0.1 | 0.5 | %/V |
| | | | SE556 | | 0.05 | 0.2 | |
| | | Each timer, astable(3) | NA556, NE556, SA556 | | 0.3 | | |
| | | | SE556 | | 0.15 | | |
| | | Timer 1 – Timer 2 | NA556, NE556, SA556 | | ±0.2 | | |
| | | | SE556 | | ±0.1 | | |
| $t_r$ | Output pulse rise time | $C_L$ = 15pF, $T_A$ = 25°C, 20% to 80% | NA556, NE556, SA556 | | 100 | 300 | ns |
| | | | SE556 | | 100 | 200 | |
| $t_f$ | Output pulse fall time | $C_L$ = 15pF, $T_A$ = 25°C, 80% to 20% | NA556, NE556, SA556 | | 100 | 300 | ns |
| | | | SE556 | | 100 | 200 | |

(1) For conditions shown as MIN or MAX, use the appropriate value specified under *Recommended Operating Conditions*.
(2) Values specified are for a device in a monostable circuit similar to Figure 6-2, with the following component values: $R_A$ = 2kΩ to 100kΩ, $C_T$ = 0.1μF.
(3) Values specified are for a device in an astable circuit similar to Figure 6-3, with the following component values: $R_A$ = 1kΩ to 100kΩ, $C_T$ = 0.1μF.

# 6 Detailed Description

## 6.1 Overview

The Nx556 or Sx556 is a precision timing device used for general-purpose timing applications. In the time-delay or monostable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle can be controlled independently with two external resistors and a single external capacitor. RESET overrides TRIG, which overrides THRES (when CONT pin is 2/3 $V_{CC}$).

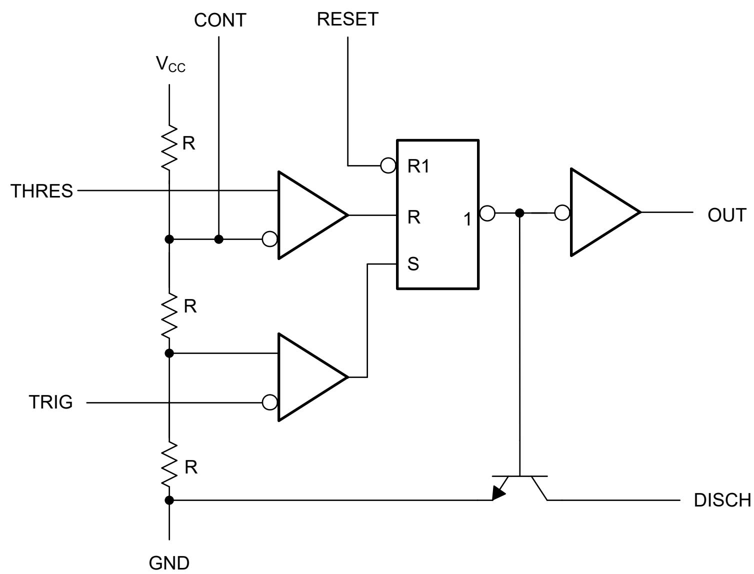
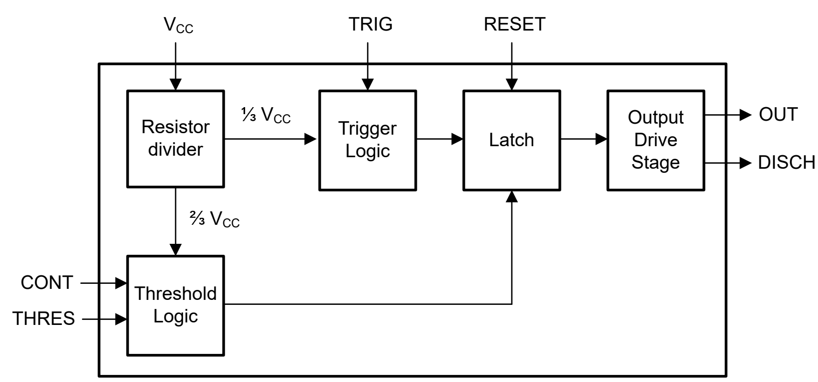



**Figure 6-1. Simplified Schematic**

## 6.2 Functional Block Diagram



## 6.3 Feature Description

### 6.3.1 Monostable Operation

For monostable operation, Figure 6-2 shows how either of the timers can be connected. If the output is low, application of a negative-going pulse to the trigger (TRIG) sets the internal latch; the output goes high, and discharge pin (DISCH) becomes open drain. Capacitor $C_T$ then is charged through $R_A$ until the voltage across the capacitor reaches the threshold voltage of the threshold (THRES) input. If TRIG has returned to a high level, the output of the threshold comparator resets the internal latch, the output goes low, the discharge pin goes low, which quickly discharges capacitor $C_T$.

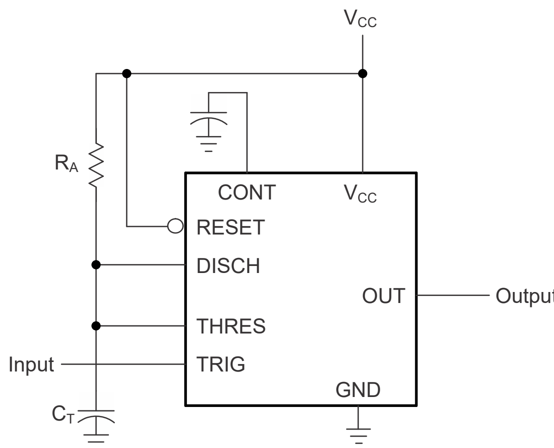



**Figure 6-2. Circuit for Monostable Operation**

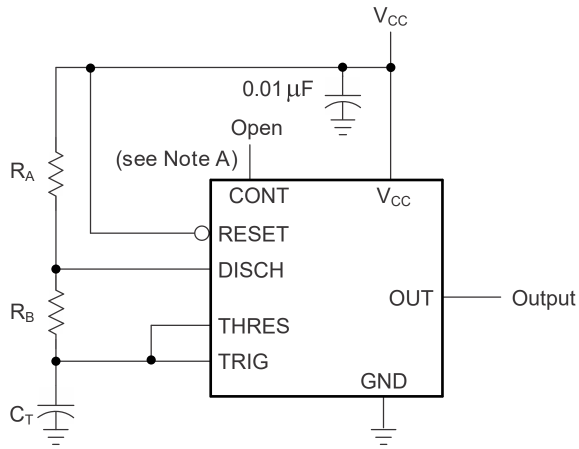
Monostable operation is initiated when TRIG voltage is less than the trigger threshold. If initiated, the sequence ends only if TRIG is high for at least 10µs before the end of the timing interval. When the trigger is grounded, the comparator storage time can be as long as 10µs, which limits the minimum monostable pulse duration to 10µs. The output pulse duration is approximately $t_w = 1.1 \times R_A C_T$. The threshold levels and charge rates both are directly proportional to the supply voltage, $V_{CC}$. The timing interval is, therefore, independent of the supply voltage, so long as the supply voltage is constant during the time interval. In monostable applications, set the trip point of the trigger input by a voltage applied to CONT.

Applying a negative-going trigger pulse simultaneously to RESET and TRIG during the timing interval discharges capacitor $C_T$ and reinitiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, when RESET is not asserted low, connect RESET to $V_{CC}$. If the RESET function is required and the pin is driven by external logic or a microcontroller, use a pullup resistor to $V_{CC}$ (such as 10kΩ) to prevent the RESET pin from floating. If the RESET function is not required, short the RESET pin directly to the $V_{CC}$ pin.

### 6.3.2 Astable Operation

As shown in Figure 6-3, adding a second resistor, $R_B$, to the circuit of Figure 6-2 and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multivibrator. The capacitor $C_T$ charges through $R_A$ and $R_B$ and then discharges through $R_B$ only. Therefore, the duty cycle is controlled by the values of $R_A$ and $R_B$.

This astable connection results in capacitor $C_T$ charging and discharging between the threshold-voltage level ($\cong 0.67 \times V_{CC}$) and the trigger-voltage level ($\cong 0.33 \times V_{CC}$). As in the monostable circuit, charge and discharge times (and, therefore, the frequency and duty cycle) are independent of the supply voltage. To reduce distortion, use at maximum frequency of 100kHz or below. If higher-frequency operation is required, consider using the TLC556 LinCMOS™ Timer instead.




Decouple CONT voltage to ground with a capacitor to improve operation. Reevaluate for individual applications.

**Figure 6-3. Circuit for Astable Operation**

$$t_H \cong 0.693 \times (R_A + R_B) \times C_T \tag{1}$$

$$t_L \cong 0.693 \times R_B \times C_T \tag{2}$$

Other useful relationships for period, frequency, and driver-referred and waveform-referred duty cycle are shown as follows:

$$T = t_H + t_L \cong 0.693 \times (R_A + 2R_B) \times C_T \tag{3}$$

$$f = \frac{1}{T} \cong \frac{1.44}{(R_A + 2R_B) \times C_T} \tag{4}$$

$$\text{Output driver duty cycle} = \frac{t_L}{T} \cong \frac{R_B}{R_A + 2R_B} \tag{5}$$

$$\text{Output waveform duty cycle} = \frac{t_H}{T} \cong 1 - \frac{R_B}{R_A + 2R_B} = \frac{R_A + R_B}{R_A + 2R_B} \tag{6}$$

## 6.4 Device Functional Modes

Table 6-1 shows the device truth table. For a valid reset voltage condition, use an external pullup resistor to $V_{CC}$ (if using the RESET functionality), or short the RESET pin directly to $V_{CC}$ (if the RESET functionality is not used).

**Table 6-1. Function Table**

| RESET VOLTAGE(1) | TRIGGER VOLTAGE(1) | THRESHOLD VOLTAGE(1) | OUTPUT | DISCHARGE SWITCH |
|---|---|---|---|---|
| LOW | Irrelevant | Irrelevant | Low | On |
| > MAX | < 1/3 × $V_{CC}$ | Irrelevant(2) | High | Off |
| > MAX | > 1/3 × $V_{CC}$ | > 2/3 × $V_{CC}$ | Low | On |
| > MAX | > 1/3 × $V_{CC}$ | < 2/3 × $V_{CC}$ | As previously established | |

(1) Voltage levels shown are nominal.
(2) CONT pin open or 2/3 × $V_{CC}$.

# 7 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

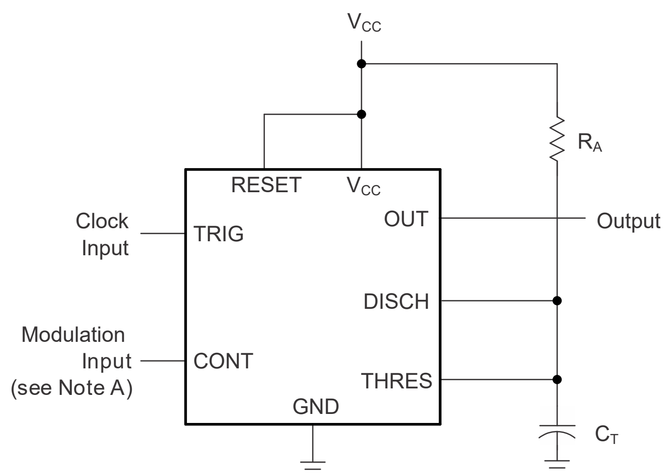
## 7.1 Application Information

The Nx556 and Sx556 timer devices use resistor and capacitor charging delay to provide a programmable time delay or operating frequency. The following sections present a simplified discussion of the design process. Reset mode forces output and discharge low and provides a small reduction in supply current.

## 7.2 Typical Applications

### *7.2.1 Pulse-Width Modulation*

To modify timer operation, apply an external voltage (or current) to CONT to modulate the internal threshold and trigger voltages. Figure 7-1 shows a circuit for pulse-width modulation. A continuous input pulse train triggers the monostable circuit, and a control signal modulates the threshold voltage. Figure 7-2 shows the resulting duty cycle versus control voltage transfer function. Attempting to run under 10% duty cycle can result in inconsistent output pulses. Attempting to run close to 100% duty cycle results in frequency division by 2, then 3, then 4.




A. The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, consider the effects of modulation source voltage and impedance on the bias of the timer.

**Figure 7-1. Circuit for Pulse-Width Modulation**

#### 7.2.1.1 Design Requirements

The clock input must have $V_{OL}$ and $V_{OH}$ levels that are less than and greater than 1/3 $V_{CC}$, respectively. Clock input $V_{OL}$ time must be less than minimum output high time; therefore, a high (positive) duty cycle clock is recommended. Minimum recommended modulation voltage is 1V. Lower CONT voltage can greatly increase threshold comparator propagation delay and storage time. The application must be tolerant of a nonlinear transfer function; the relationship between modulation input and pulse width is not linear because the capacitor charge is RC-based with an negative exponential curve.

#### 7.2.1.2 Detailed Design Procedure

Choose $R_A$ and $C_T$ so that $R_A \times C_T$ is same or less than clock input period. Figure 7-2 shows the non linear relationship between control voltage and output duty cycle. Duty cycle is function of control voltage and clock period relative to RC time constant.

#### 7.2.1.3 Application Curve

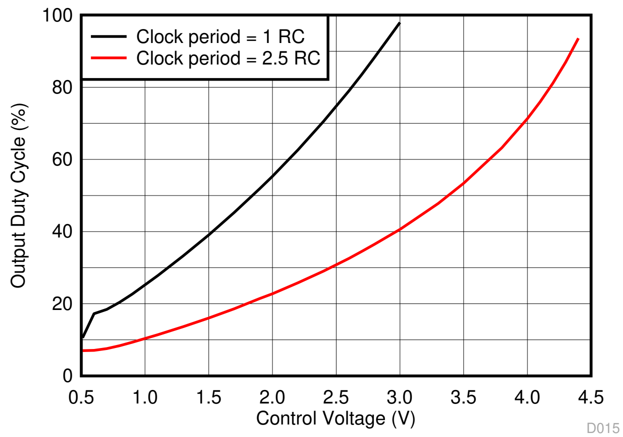
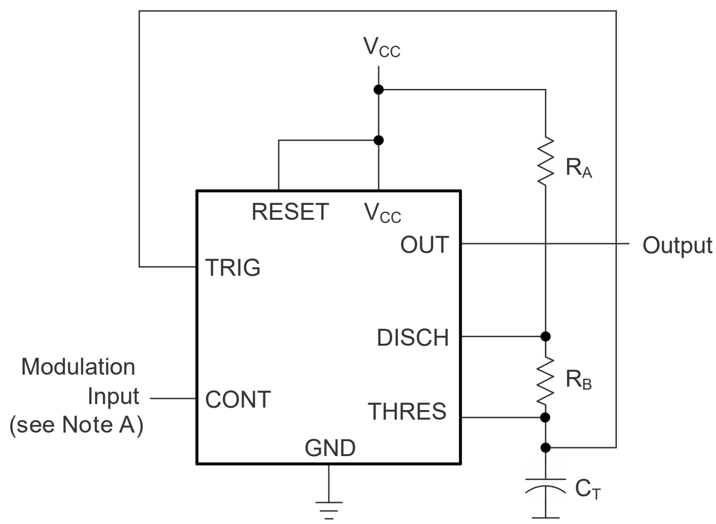



**Figure 7-2. Pulse-Width-Modulation vs Control Voltage Clock Duty Cycle 98%, $V_{CC}$ = 5V**

### *7.2.2 Pulse-Position Modulation*

Figure 7-3 shows that any of these timers can be used as a pulse-position modulator. This application modulates the threshold voltage, and thereby, the time delay of a free-running oscillator. Figure 7-4 and Figure 7-5 show the output frequency and duty cycle versus control voltage.




A. The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, consider the effects of modulation source voltage and impedance on the bias of the timer.

**Figure 7-3. Circuit for Pulse-Position Modulation**

#### 7.2.2.1 Design Requirements

Both dc- and ac-coupled modulation input changes the upper and lower voltage thresholds for the timing capacitor. Both frequency and duty cycle vary with the modulation voltage. Control voltage less than 1V can result in output glitches instead of a steady-output pulse stream. Table 7-1 gives example design requirements.

**Table 7-1. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| $R_A$ | 3kΩ |
| $R_B$ | 309Ω |
| $C_T$ | 1nF |

#### 7.2.2.2 Detailed Design Procedure

The nominal output frequency and duty cycle for control voltage set to 2/3 of $V_{CC}$ can be determined using formulas in *Section 6.3.2*.

#### 7.2.2.3 Application Curves

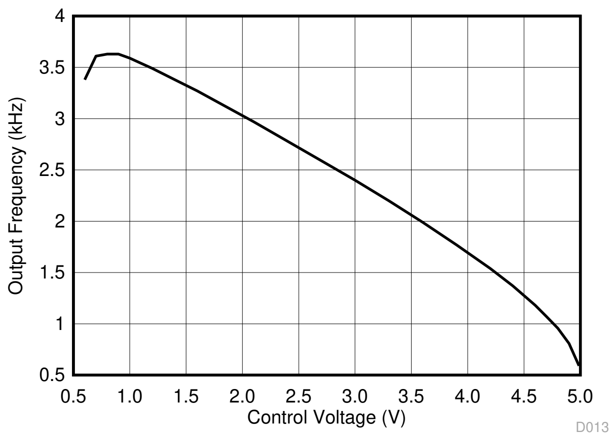



**Figure 7-4. Pulse-Position-Modulation Frequency vs Control Voltage, $V_{CC}$ = 5V**

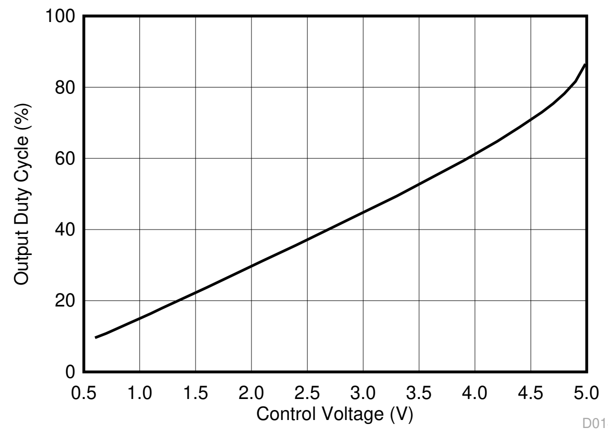



**Figure 7-5. Pulse-Position-Modulation Duty Cycle vs Control Voltage, $V_{CC}$ = 5V**

# 8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

# 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision H (December 2024) to Revision I (March 2025)** **Page**

- Updated *Device Information* table to show correct temperature range for each device....................................1
- Added thermal specifications for DB package in *Thermal Information* ............................................................3
- Changed minimum monostable pulse duration from 1μs to 10μs in *Monostable Operation* to fix typo.............8

**Changes from Revision G (June 2006) to Revision H (December 2024)** **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document................. 1
- Added *Pin Configuration and Functions*, *Specifications*, *Detailed Description*, *Application and Implementation*, *Device and Documentation Support* sections and associated subsections...................................................... 1
- Updated *Description*, *Applications*, and *Features* sections................................................................................ 1
- Added DB package to data sheet.........................................................................................................................1
- Deleted package thermal information and related footnotes from *Absolute Maximum Ratings* .........................3
- Added *ESD Ratings* table and HBM and CDM specifications.............................................................................3
- Deleted redundant input voltage ($V_I$) specification in *Recommended Operating Conditions* ............................ 3
- Changed *Power Dissipation Ratings* table to *Thermal Information*, and updated per-package thermal specifications............................................................................................................................. 3
- Changed *Operating Characteristics* title to *Switching Characteristics*, and clarified that values are specified by design or characterization and are not production tested...................................................................6

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| JM38510/10902BCA | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510 /10902BCA |
| JM38510/10902BCA.A | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510 /10902BCA |
| NA556D | Obsolete | Production | SOIC (D) \| 14 | - | - | Call TI | Call TI | -40 to 105 | NA556 |
| NA556DR | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | NA556 |
| NA556DR.A | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | NA556 |
| NA556N | Active | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 105 | NA556N |
| NA556N.A | Active | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 105 | NA556N |
| NE556D | Obsolete | Production | SOIC (D) \| 14 | - | - | Call TI | Call TI | 0 to 70 | NE556 |
| NE556DBR | Active | Production | SSOP (DB) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | N556 |
| NE556DBR.A | Active | Production | SSOP (DB) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | N556 |
| NE556DR | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | NE556 |
| NE556DR.A | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | NE556 |
| NE556N | Active | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | NE556N |
| NE556N.A | Active | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | NE556N |
| NE556NSR | Active | Production | SOP (NS) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | NE556 |
| NE556NSR.A | Active | Production | SOP (NS) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | NE556 |
| SA556N | Active | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SA556N |
| SA556N.A | Active | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SA556N |
| SE556J | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SE556J |
| SE556J.A | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SE556J |
| SE556JB | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SE556JB |
| SE556JB.A | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SE556JB |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

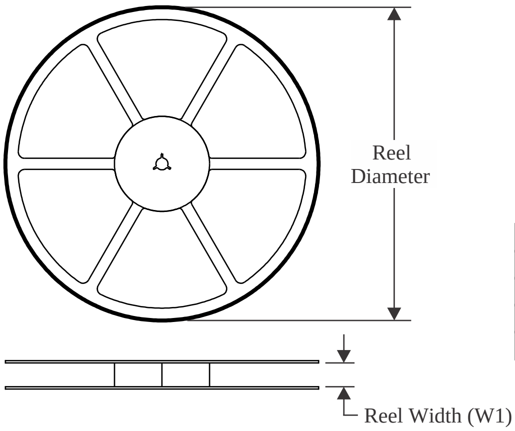
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

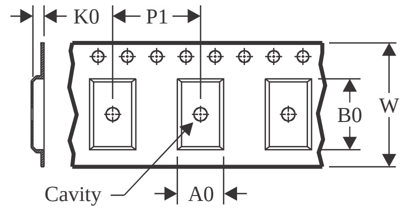
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

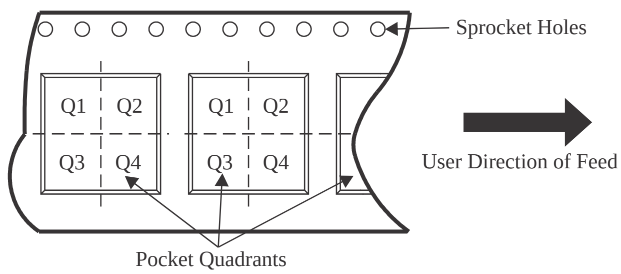



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

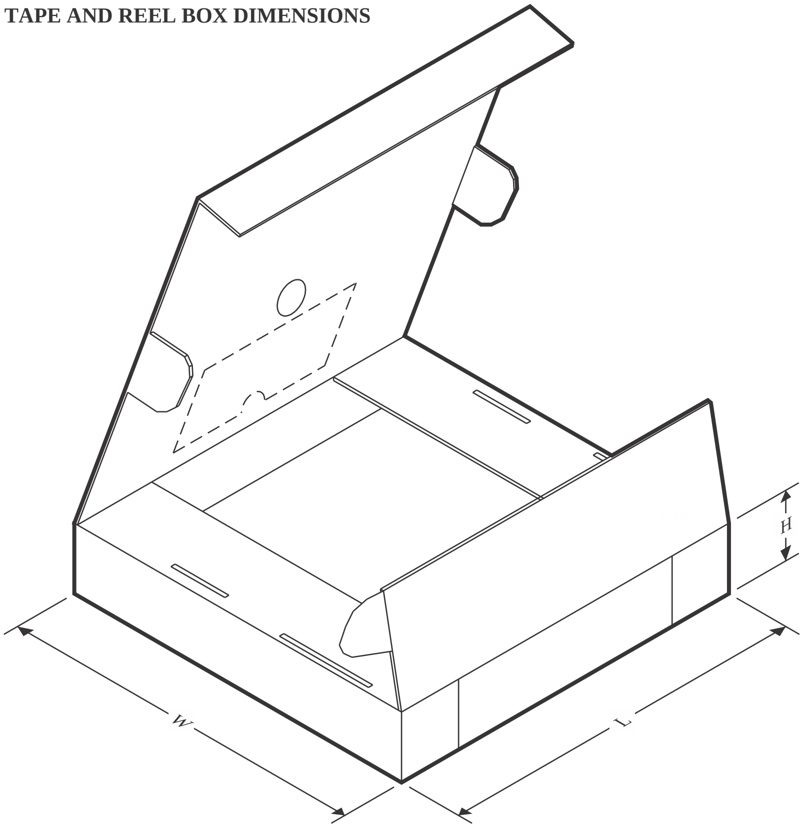
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| NA556DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| NE556DBR | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| NE556DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| NE556DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| NE556NSR | SOP | NS | 14 | 2000 | 330.0 | 16.4 | 8.1 | 10.4 | 2.5 | 12.0 | 16.0 | Q1 |

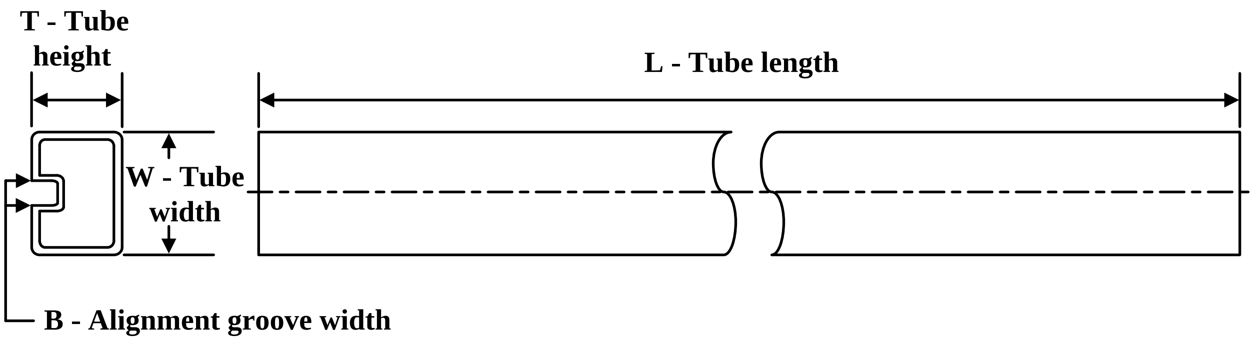
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

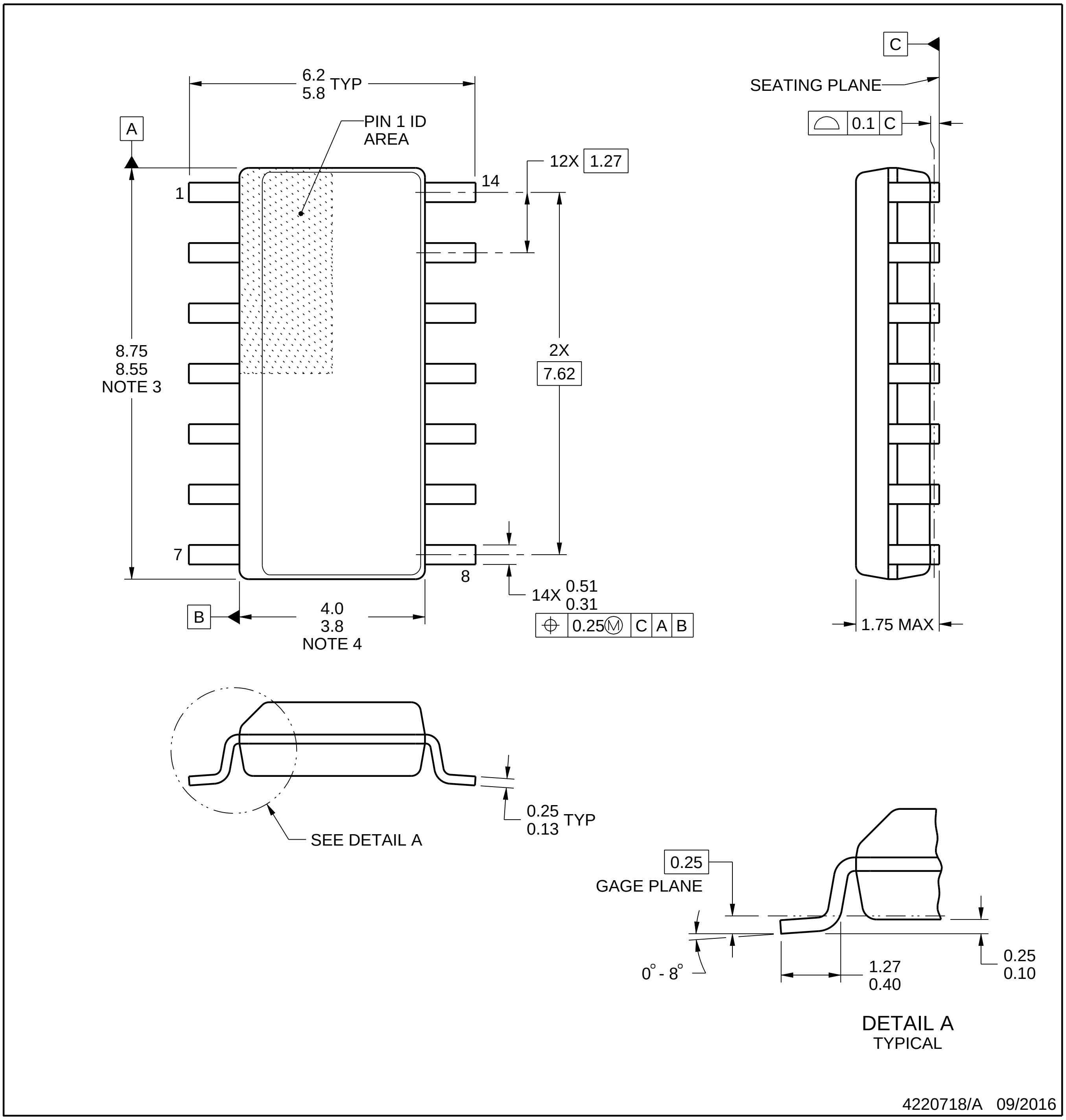
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| NA556DR | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| NE556DBR | SSOP | DB | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| NE556DR | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| NE556DR | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| NE556NSR | SOP | NS | 14 | 2000 | 353.0 | 353.0 | 32.0 |

## TUBE



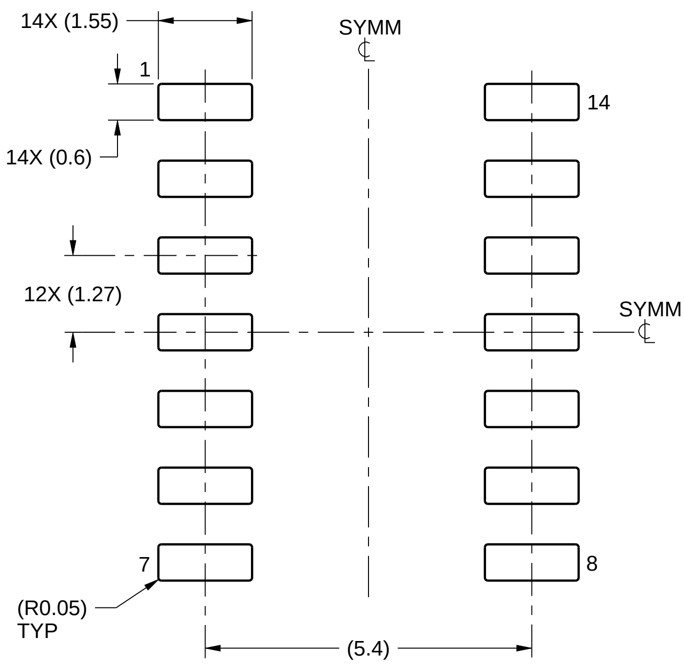

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| NA556N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| NA556N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| NA556N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| NA556N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| NE556N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| NE556N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| NE556N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| NE556N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SA556N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SA556N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |

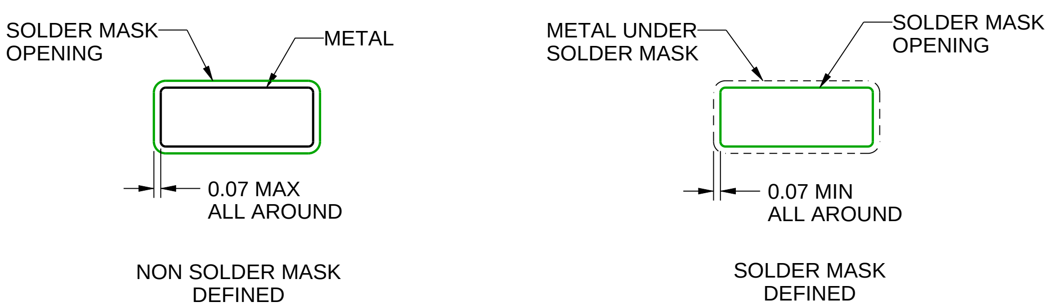



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X

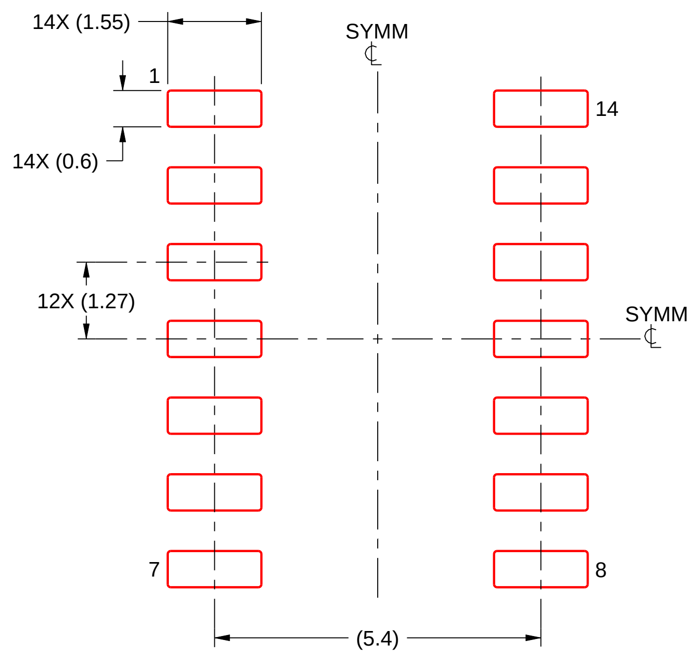



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

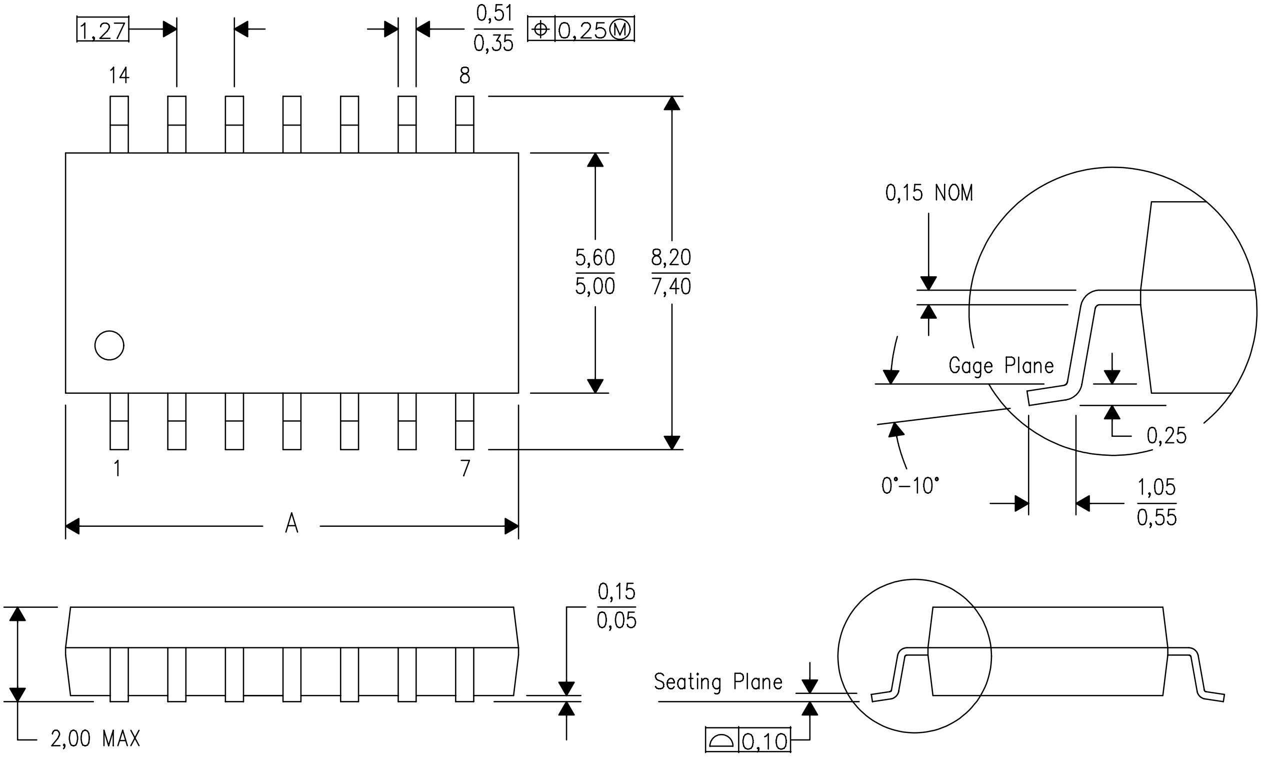
4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

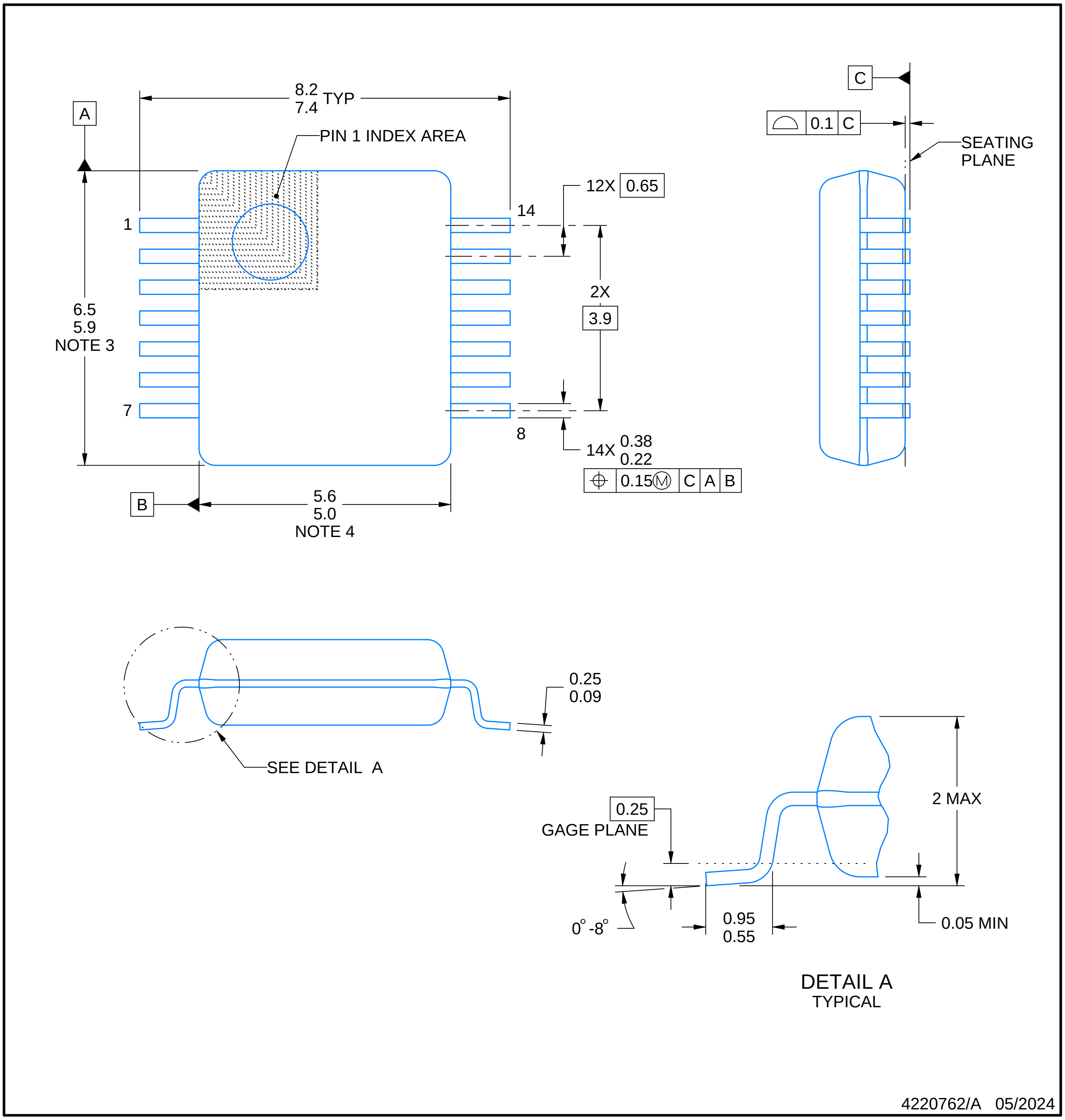
**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

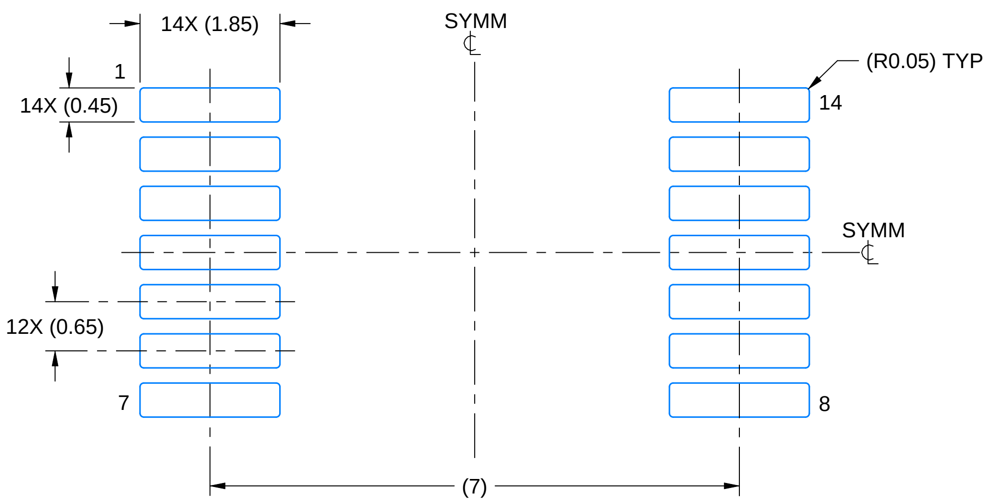
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

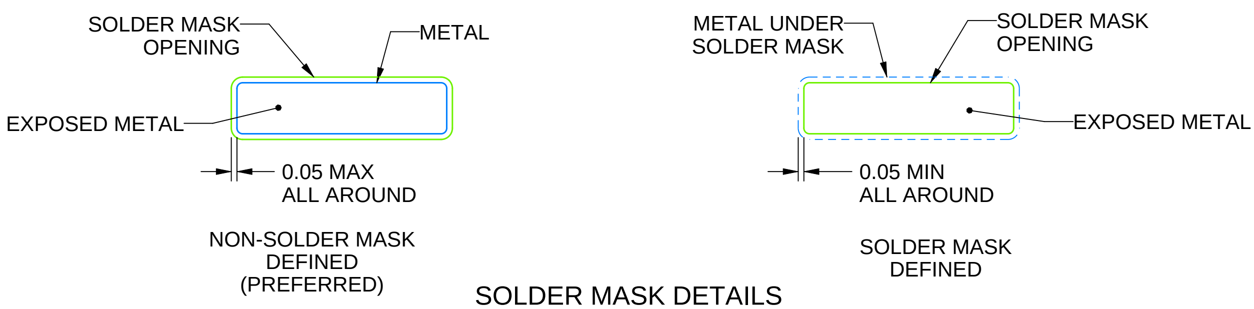



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

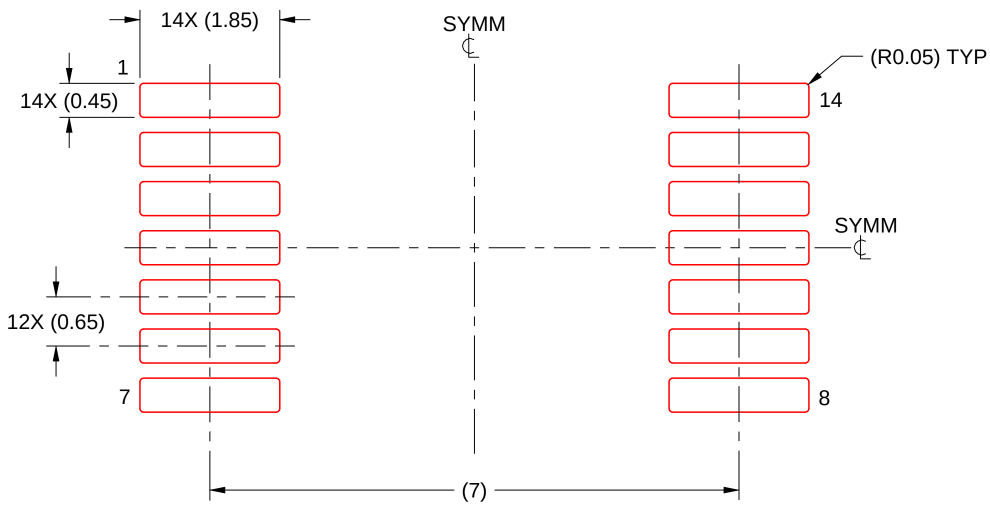



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

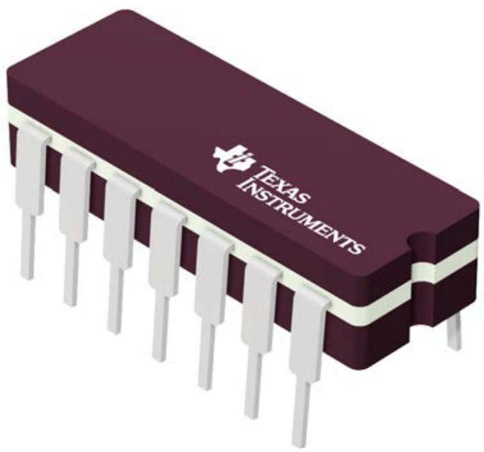
4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

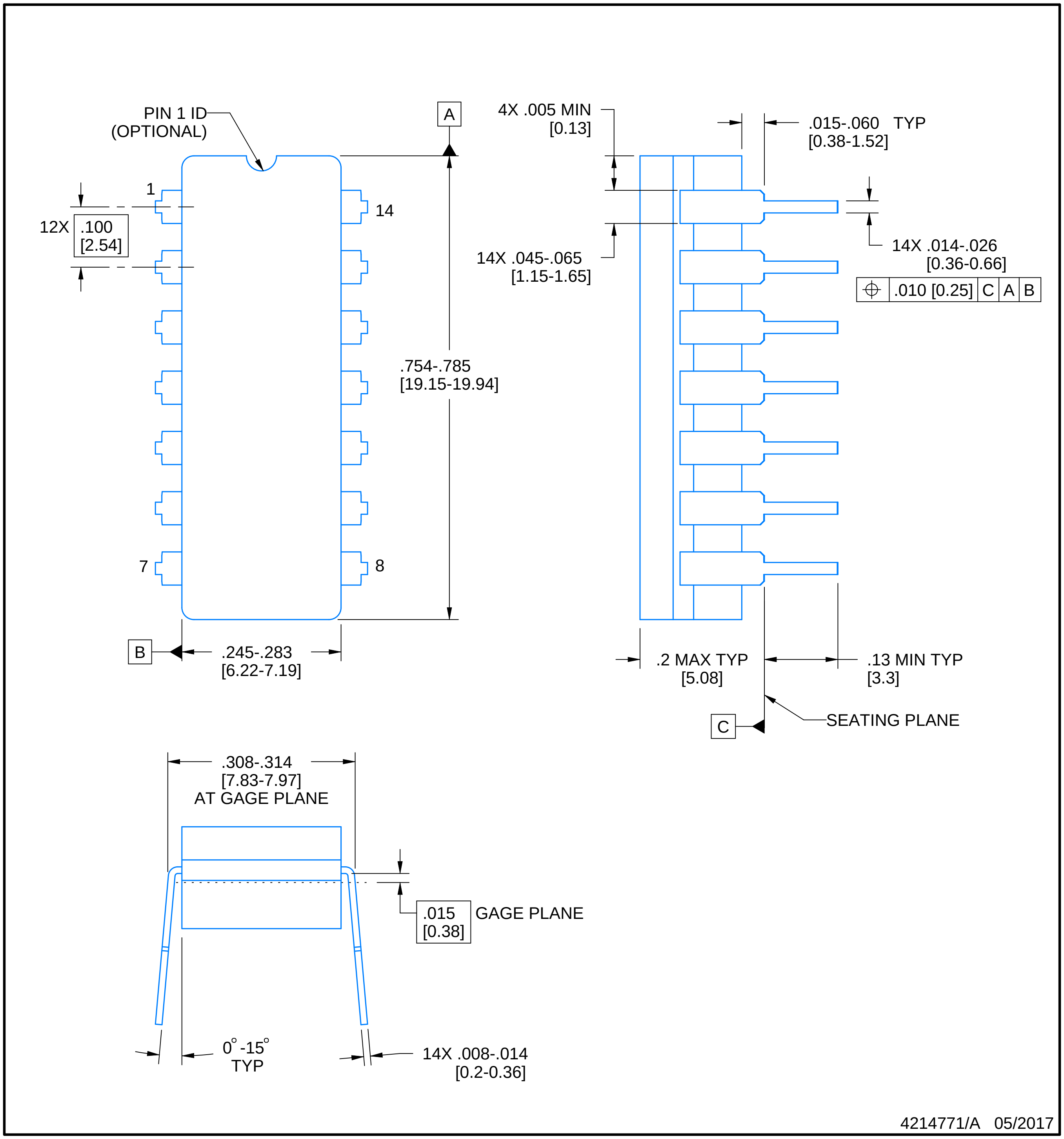
# J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



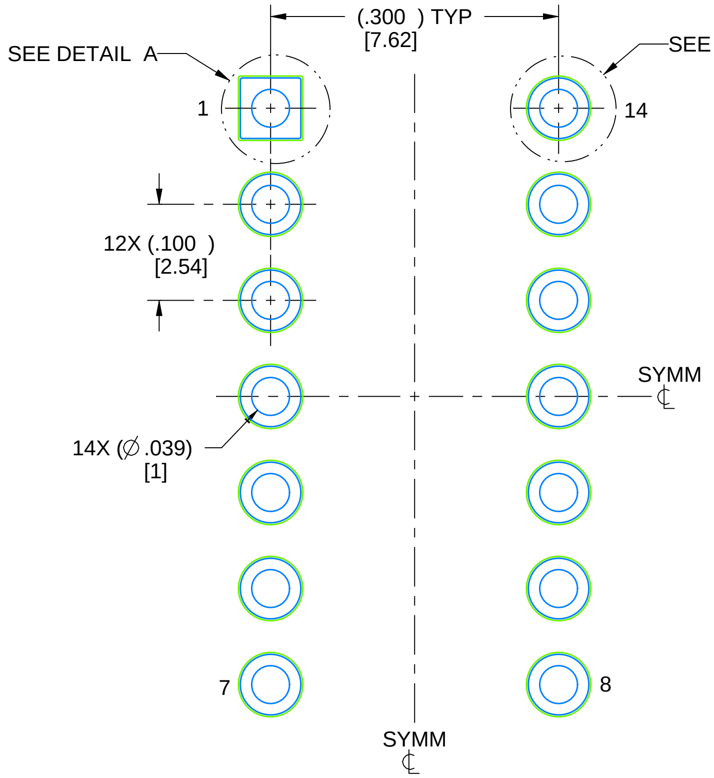

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

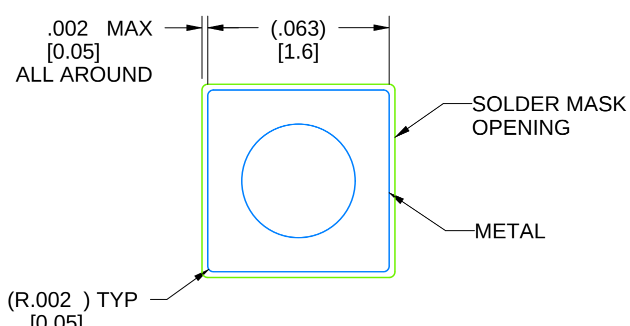



NOTES:

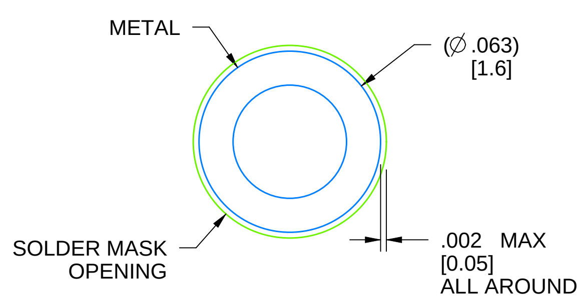
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.




LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X




DETAIL A
SCALE: 15X



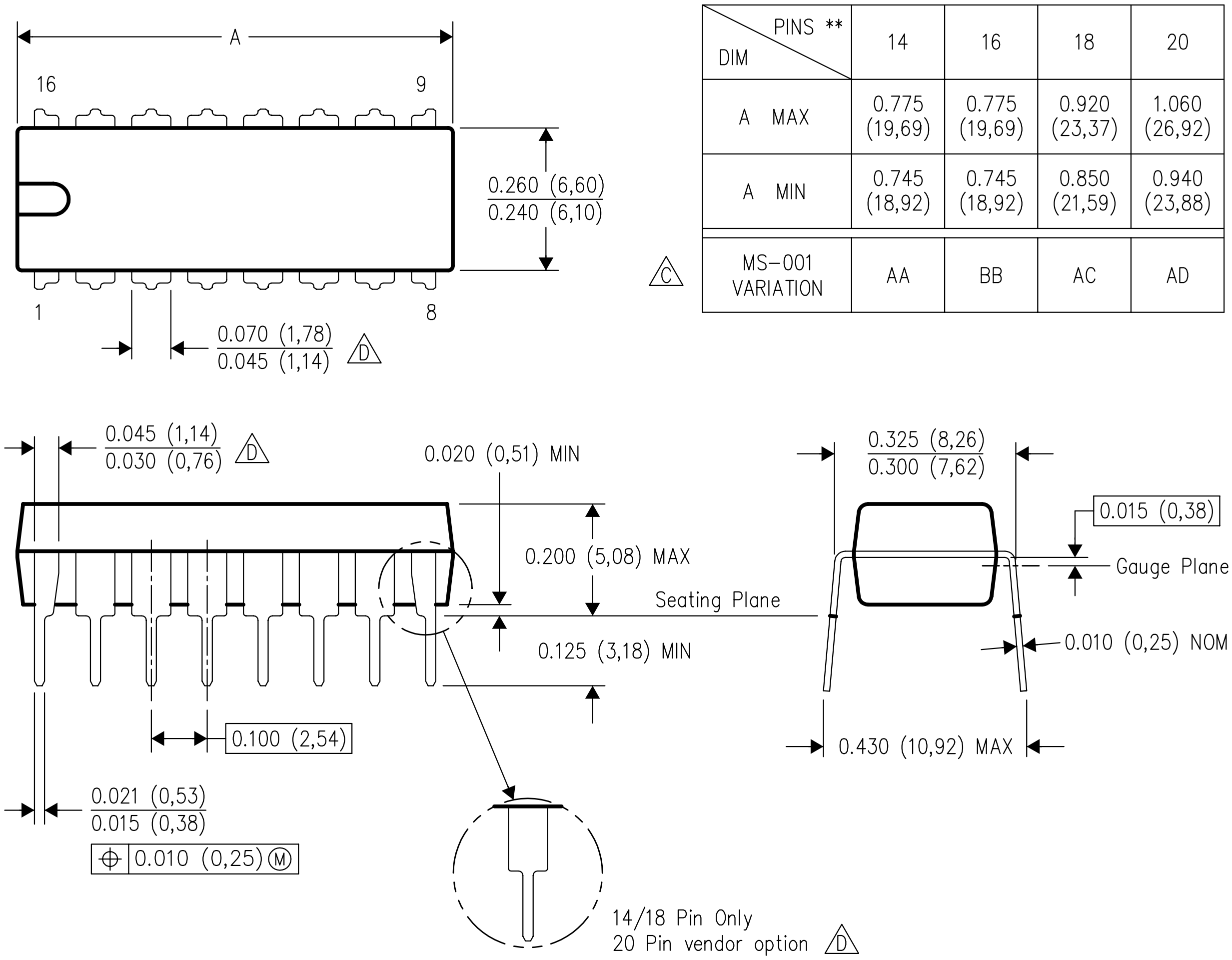

DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

## N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

| PINS ** / DIM | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| C MS–001 VARIATION | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.