BT149D

SCR

Rev.02 - 12 October 2021 Product data sheet

1. General description

Planar passivated Silicon Controlled Rectifier in a TO92 plastic package. This SCR is designed to be interfaced directly to microcontrollers, logic ICs and other low power gate trigger circuits.

2. Features and benefits

- Planar passivated for voltage ruggedness and reliability
- Sensitive gate
- Direct triggering from low power drivers and logic ICs
- A-G-K reverse pin-out

3. Applications

- General purpose switching and phase control
- Low power circuits

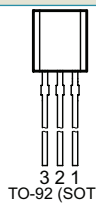
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Absolute maximum rating							
V_{RRM}	repetitive peak reverse voltage			-	-	400	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{lead} \leq 83$ °C; Fig. 1		-	-	0.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{lead} \leq 83$ °C; Fig. 2; Fig. 3		-	-	0.8	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25$ °C; $t_p = 10$ ms; Fig. 4; Fig. 5		-	-	8	A
		half sine wave; $T_{j(init)} = 25$ °C; $t_p = 8.3$ ms		-	-	9	A
T_j	junction temperature			-	-	125	°C
Static characteristics							
I_{GT}	gate trigger current	$V_D = 12$ V; $I_T = 10$ mA; $T_j = 25$ °C; Fig. 7		-	50	200	µA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 268$ V; $T_j = 125$ °C; $R_{GK} = 1$ kΩ; (V_{DM} = 67% of V_{DRM}); exponential waveform; Fig. 12		500	800	-	V/µs
		$V_{DM} = 268$ V; $T_j = 125$ °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 12		-	25	-	V/µs

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 TO-92 (SOT54)	 *sym037*
2	G	gate		
3	A	anode		

6. Ordering information

Table 3. Ordering information

Type number	Package Name	Orderable part number	Packing method	Small packing quantity	Package version	Package issue date
BT149D	TO92	BT149D,126	Reel	2000	SOT54 wide pitch	14-Nov-2013
BT149D	TO92	BT149D,112	Bulk	1000	SOT54	14-Nov-2013

7. Marking

Table 4. Marking codes

Type number	Marking codes
BT149D	BT149D

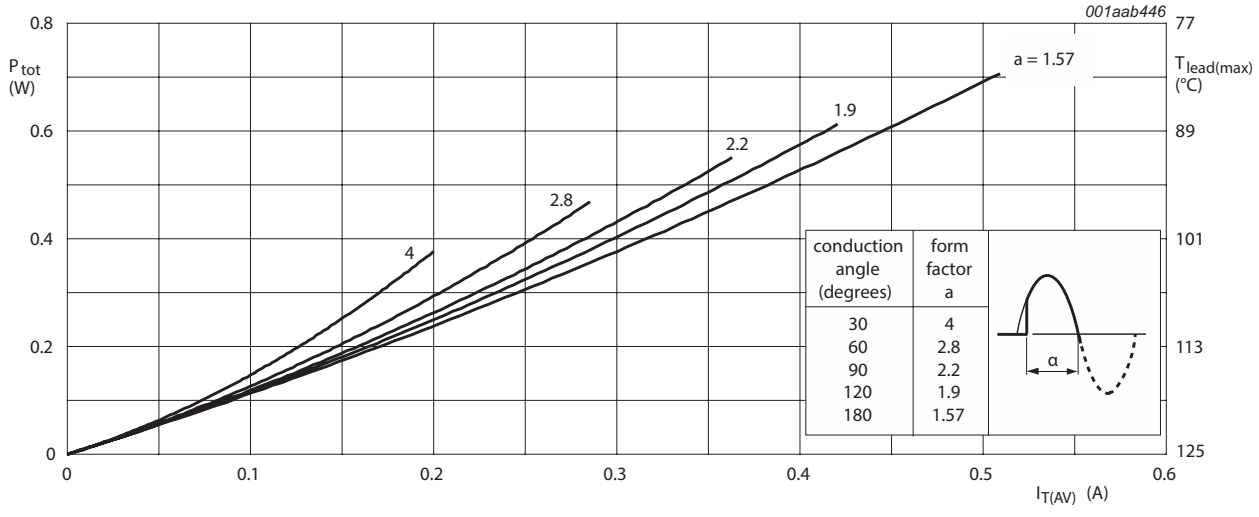
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	400	V
V_{RRM}	repetitive peak reverse voltage			-	400	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{lead} \leq 83$ °C; Fig. 1		-	0.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{lead} \leq 83$ °C; Fig. 2; Fig. 3		-	0.8	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25$ °C; $t_p = 10$ ms; Fig. 4; Fig. 5		-	8	A
		half sine wave; $T_{j(init)} = 25$ °C; $t_p = 8.3$ ms		-	9	A
I^2t	I^2t for fusing	$t_p = 10$ ms; SIN		-	0.32	A^2s
dI_T/dt	rate of rise of on-state current	$I_T = 2$ A; $I_G = 10$ mA; $dI_G/dt = 100$ mA/µs		-	50	A/µs
I_{GM}	peak gate current			-	1	A
V_{RGM}	peak reverse gate voltage			-	5	V
P_{GM}	peak gate power			-	2	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.1	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature		[1]	-	125	°C

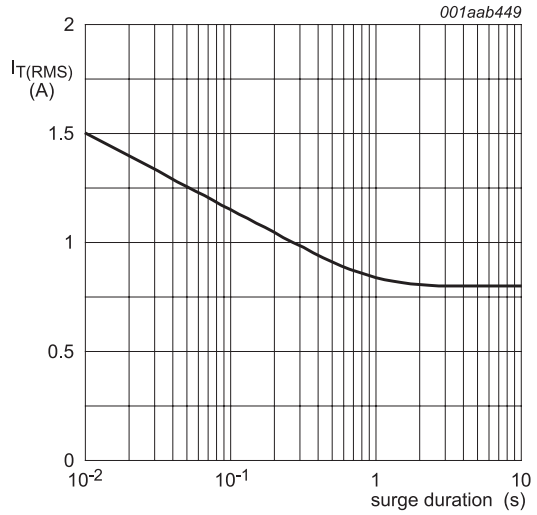
[1] Operation above 110˚C may require the use of a gate to cathode resistor of 1kΩ or less.



a = form factor = $I_{T(RMS)} / I_{T(AV)}$

α = conduction angle

Fig. 1. Total power dissipation as a function of average on-state current; maximum values



f = 50 Hz; T_{lead} = 83 °C

Fig. 2. RMS on-state current as a function of surge duration for sinusoidal currents

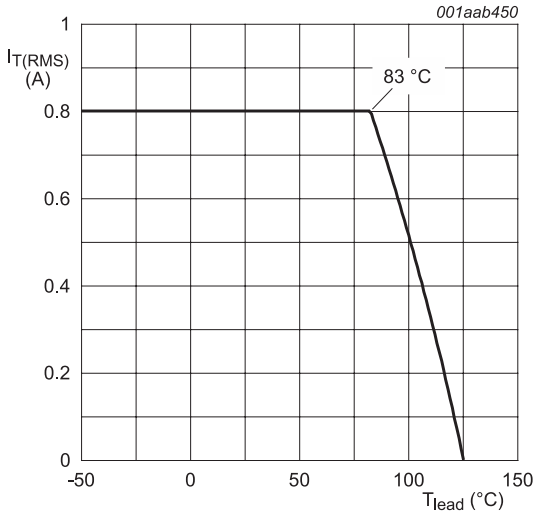
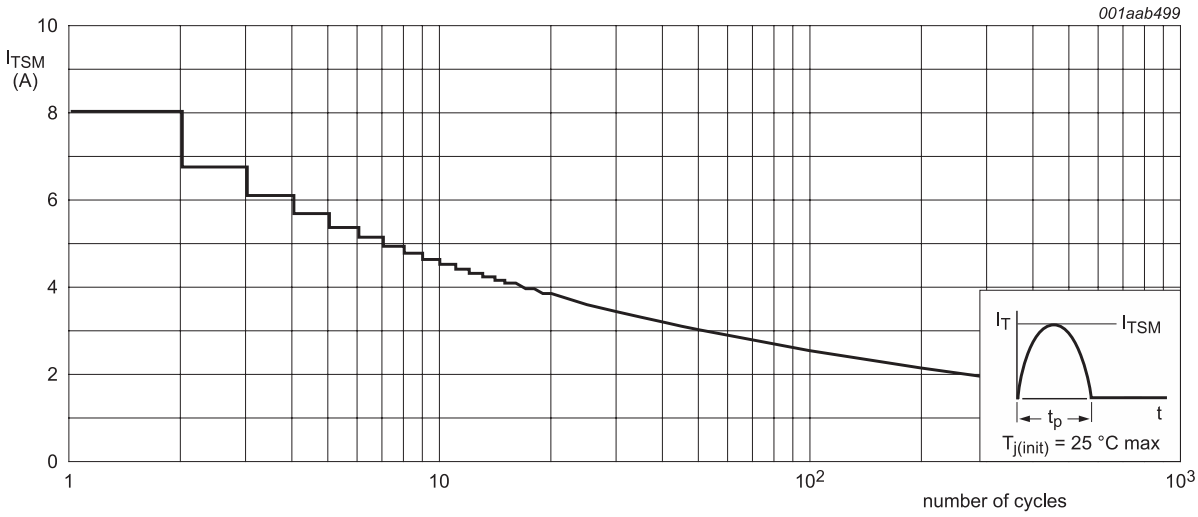
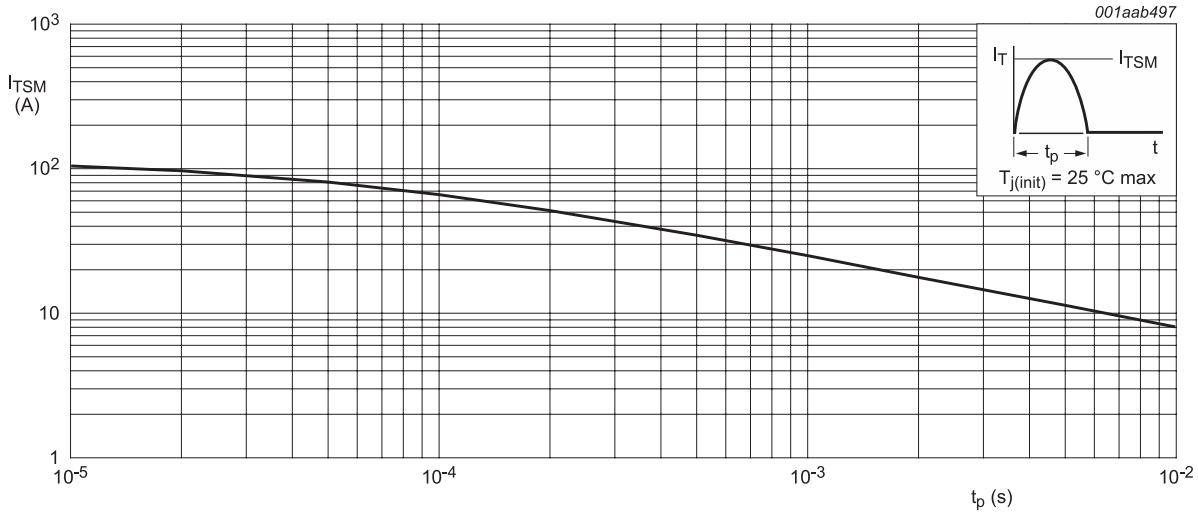


Fig. 3. RMS on-state current as a function of lead temperature; maximum values



f = 50 Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal currents cycles; maximum values



$t_p \leq 10$ ms

Fig. 5. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j\text{-}lead)}$	thermal resistance from junction to lead	Fig. 6		-	-	60	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient free air	printed circuit board mounted: lead length = 4 mm		-	150	-	K/W

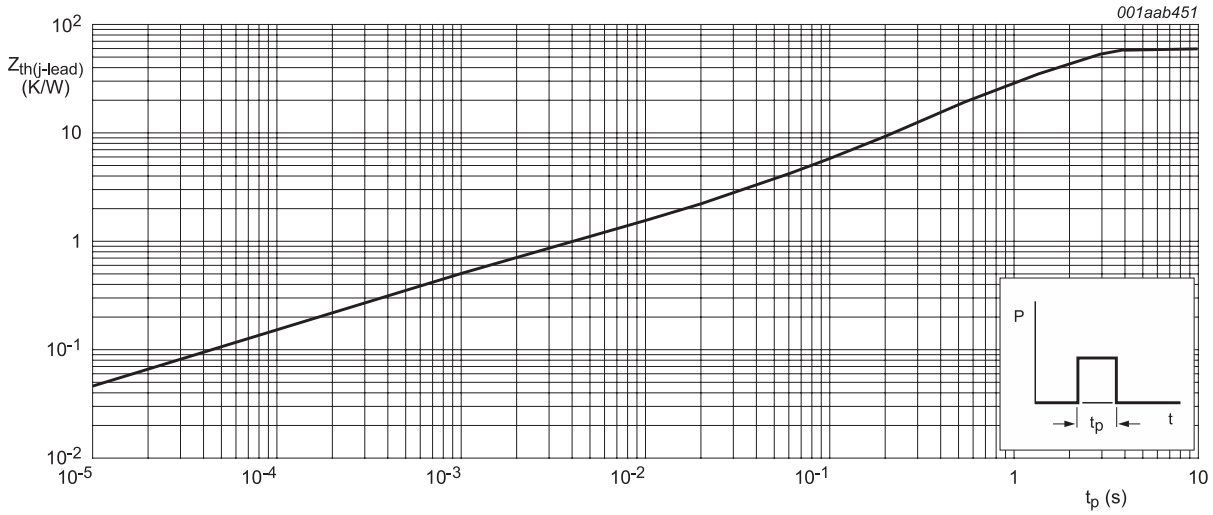


Fig. 6. Transient thermal impedance from junction to lead as a function of pulse width

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 10 mA; T_j = 25 °C; Fig. 7		-	50	200	µA
I_L	latching current	V_D = 12 V; I_G = 0.5 mA; T_j = 25 °C; $R_{GK(ext)}$ = 1 kΩ; Fig. 8		-	2	6	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; $R_{GK(ext)}$ = 1 kΩ; Fig. 9		-	2	5	mA
V_T	on-state voltage	I_T = 1.2 A; T_j = 25 °C; Fig. 10		-	1.25	1.7	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 10 mA; T_j = 25 °C; Fig. 11		-	0.5	0.8	V
		V_D = 400 V; I_T = 10 mA; T_j = 125 °C		0.2	0.3	-	V
I_D	off-state current	V_D = 400 V; $R_{GK(ext)}$ = 1 kΩ; T_j = 125 °C		-	0.05	0.1	mA
I_R	reverse current	V_R = 400 V; T_j = 125 °C; $R_{GK(ext)}$ = 1 kΩ		-	0.05	0.1	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 268 V; T_j = 125 °C; R_{GK} = 1 kΩ; (V_{DM} = 67% of V_{DRM}); exponential waveform; Fig. 12		500	800	-	V/µs
		V_{DM} = 268 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 12		-	25	-	V/µs
t_{gt}	gate-controlled turn-on time	I_{TM} = 2 A; V_D = 400 V; I_G = 10 mA; dI_G/dt = 0.1 A/µs; T_j = 25 °C		-	2	-	µs
t_q	commutated turn-off time	V_{DM} = 268 V; T_j = 125 °C; I_{TM} = 1.6 A; V_R = 35 V; $(dI_T/dt)_M$ = 30 A/µs; dV_D/dt = 2 V/µs; $R_{GK(ext)}$ = 1 kΩ; (V_{DM} = 67% of V_{DRM})		-	100	-	µs

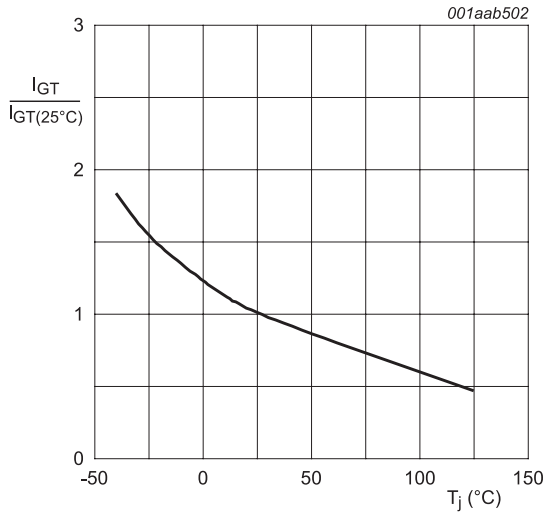
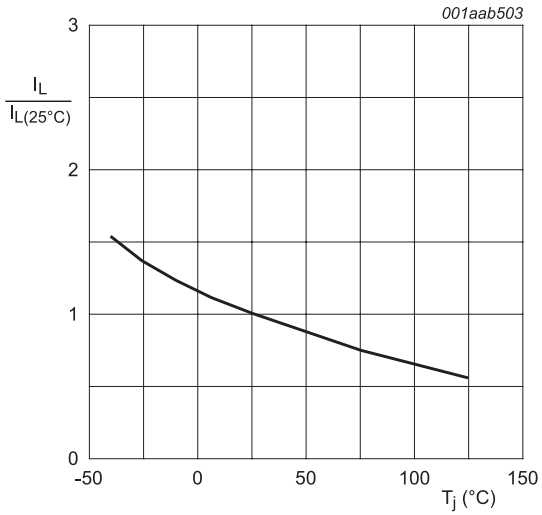
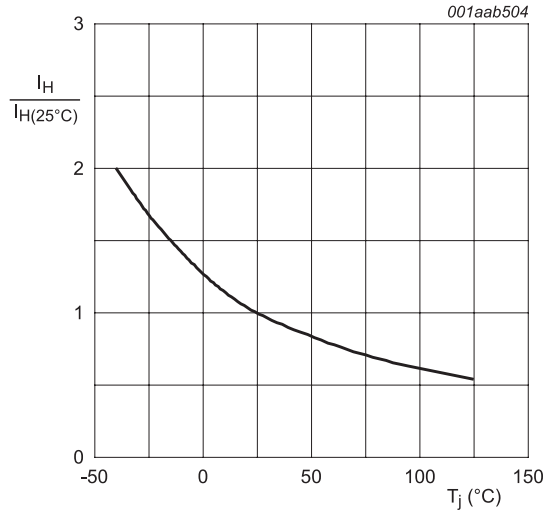


Fig. 7. Normalized gate trigger current as a function of junction temperature



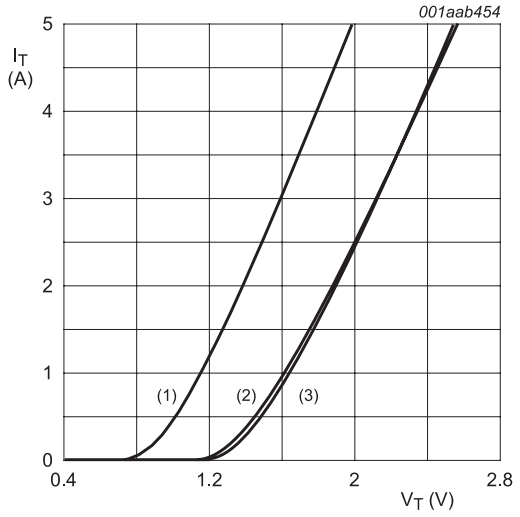
R_{GK} = 1 kΩ

Fig. 8. Normalized latching current as a function of junction temperature



R_{GK} = 1 kΩ

Fig. 9. Normalized holding current as a function of junction temperature



V_o = 1.067 V; R_s = 0.187 Ω
(1) T_j = 125 °C; typical values
(2) T_j = 125 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

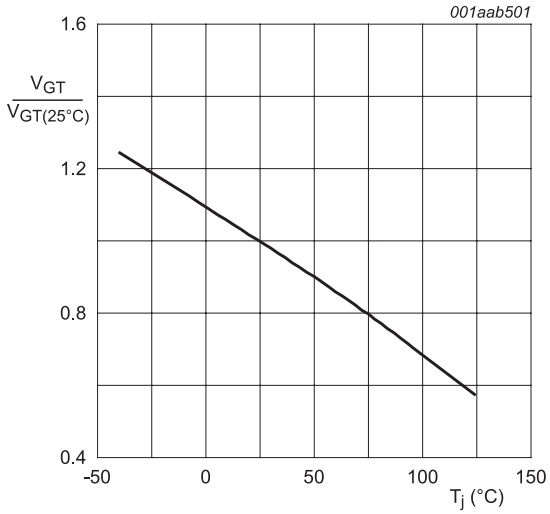
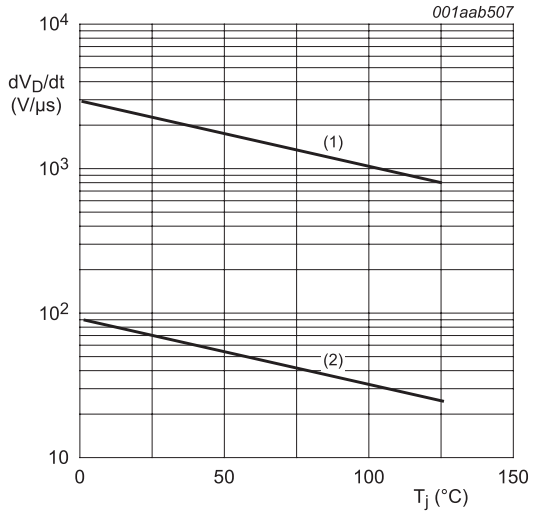


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

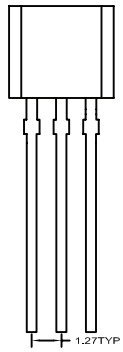


(1) R_{GK} = 1 kΩ;
(2) gate open circuit

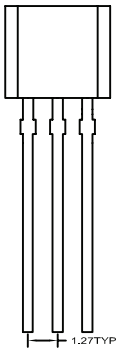
Fig. 12. Critical rate of rise of off-state voltage as a function of junction temperature; typical values

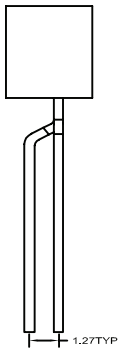
11. Package outline

SOT54 PACKAGE OUTLINE

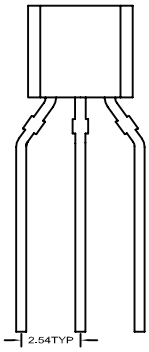


SOT54
Bulk Pack - 412

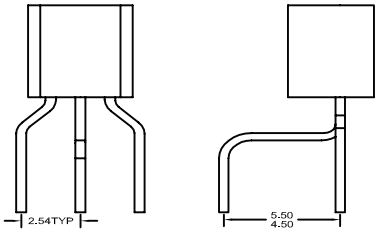




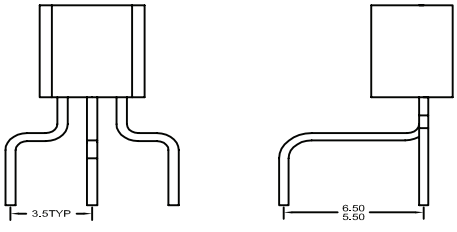
SOT54 LEADS ON CIRCLE
Bulk Pack - 112



SOT54 WIDE PITCH
Tape/ Reel Pack - 116
Ammo Pack - 126



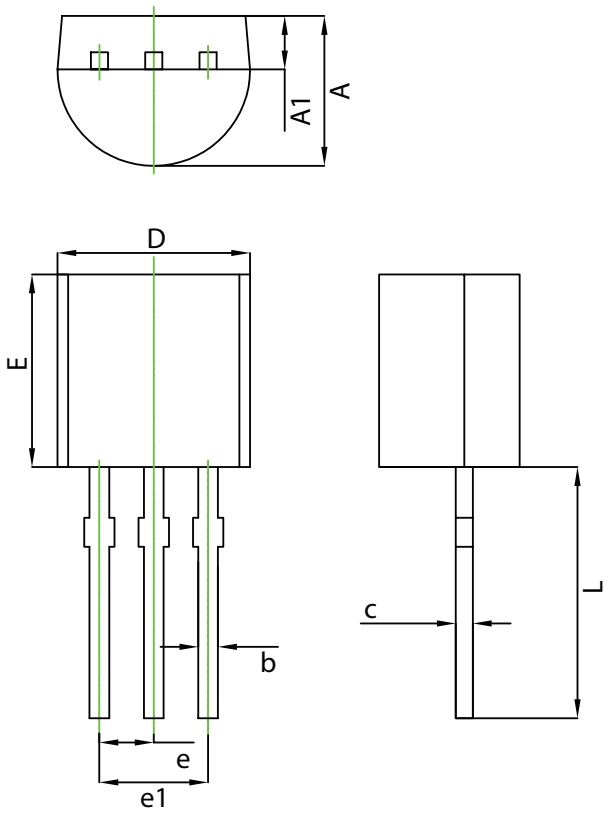
SOT54 LEAD BEND L01
Bulk Pack - 412



SOT54 LEAD BEND L02
Bulk Pack - 412

Remark: Detailed dimensions refer to POD drawing.

Plastic single-ended leaded(through hole) package; 3 leads TO92



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.300	3.700	0.130	0.146
A1	1.100	1.400	0.043	0.055
b	0.380	0.550	0.015	0.022
c	0.360	0.510	0.014	0.020
D	4.300	4.700	0.169	0.185
E	4.300	4.700	0.169	0.185
e	1.270 TYP.		0.050 TYP.	
e1	2.440	2.640	0.096	0.104
L	14.100	14.500	0.555	0.571

12. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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13. Contents

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Date of release: 12 October 2021