UMW NDT3055L

60V N-Channel MOSFET

1.Description

These logic level N-Channel enhancement This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance, and withstand high energy pulse in the avalanche and commutation modes.

2.1Features

- $V_{DS\ (V)}$=60V
- $R_{DS(ON)}$<100mΩ(V_{GS}=10V)
- $R_{DS(ON)}$<120mΩ(V_{GS}=4.5V)
- Low drive requirements allowing operation directly from logic drivers. VGS(TH) < 2V

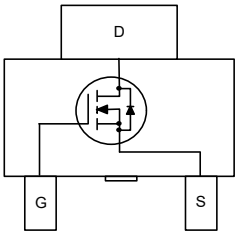
2.2Features

- High power and current handling capability in a widely used surface mount package.
- High density cell design for extremely low $R_{DS(ON)}$

3.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

SOT-223 top view



4.Absolute Maximum Ratings T_A= 25°C

Parameter		Symbol	Rating	Units
Drain-Source Voltage		V_{DSS}	60	V
Gate-Source Voltage		V_{GSS}	±20	V
Drain Current - Continuous	(Note 1a)	I_D	4	A
-Pulsed			25	A
Power Dissipation for Single Operation	(Note 1a)	P_D	3	W
	(Note 1b)		1.3	W
	(Note 1c)		1.1	W
Storage Junction Temperature Range		T_J, T_{STG}	-65 to 150	°C

5.Thermal Characteristics

Parameter		Symbol	Rating	Units
Thermal Resistance, Junction-to-Ambient	(Note 1a)	$R_{\theta JA}$	42	°C/W
Thermal Resistance, Junction-to-Case	(Note 1)	$R_{\theta JC}$	12	°C/W

Notes:

* Order option J23Z for cropped center drain lead.

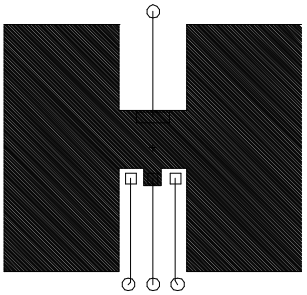
6.Electrical Characteristic (T_A=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	60			V
Breakdown Voltage Temp. Coefficient	$\Delta BV_{DSS}/\Delta T_J$	I_D=250μA Referenced to 25°C		55		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V, V_{GS}=0V			1	μA
		T_J=125°C			50	μA
Gate - Body Leakage, Forward	I_{GSSF}	V_{GS}=20V, V_{DS}=0V			100	nA
Gate - Body Leakage, Reverse	I_{GSSR}	V_{GS}=-20V, V_{DS}=0V			-100	nA
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1	1.6	2	V
Gate Threshold Voltage Temp. Coefficient	$\Delta V_{GS(th)}/T_J$	I_D=250μA Referenced to 25°C		-4		mV/°C
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=4A		70	100	mΩ
		V_{GS}=4.5V, I_D=3.7A		103	120	
On-State Drain Current	$I_{D(ON)}$	V_{GS}=5V, V_{DS}=10V	10			A
Forward Transconductance	g_{FS}	V_{DS}=5V, I_D=4A		7		S
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V, f=1MHz		345		pF
Output Capacitance	C_{oss}			110		pF
Reverse Transfer Capacitance	C_{rss}			30		pF
SWITCHING CHARACTERISTICS (Note 2)						
Turn - On Delay Time	$t_{D(on)}$	V_{DD}=25V, I_D=1A V_{GS}=10V, R_{GEN}=6Ω		5	20	ns
Turn - On Rise Time	t_r			7.5	20	ns
Turn - Off Delay Time	$t_{D(off)}$			20	50	ns
Turn - Off Fall Time	t_f			7	20	ns

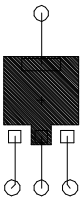
Total Gate Charge	Q_g	V_{DS}=40V, I_D=4A V_{GS}=10V		13	20	nC
Gate-Source Charge	Q_{gs}			1.7		nC
Gate-Drain Charge	Q_{gd}			3.2		nC
Drain–Source Diode Characteristics and Maximum Ratings						
Maximum Continuous Drain–Source Diode Forward Current	I_S				2.5	A
Drain–Source Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S=2.5A (Note2)		0.8	1.2	V

Notes:

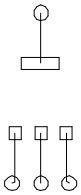
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 42°C/W when mounted on a 1 in^2 pad of 2oz Cu.



b. 95°C/W when mounted on a pad of 2oz Cu.



c. 110°C/W when mounted on a 0.00123 in^2 pad of 2oz Cu.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%.

7.1Typical characteristic

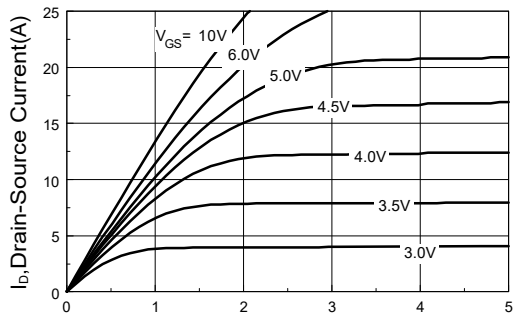


Figure 1: On-Region Characteristics

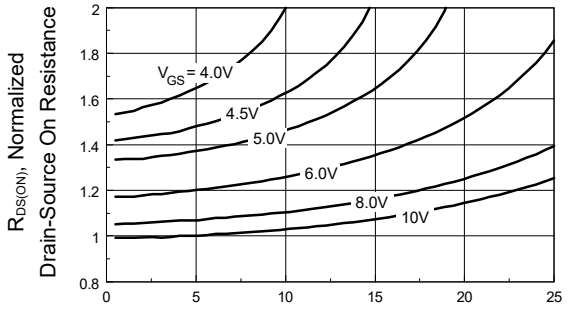


Figure 2: On-Resistance Variation with Drain Current and Gate Voltage

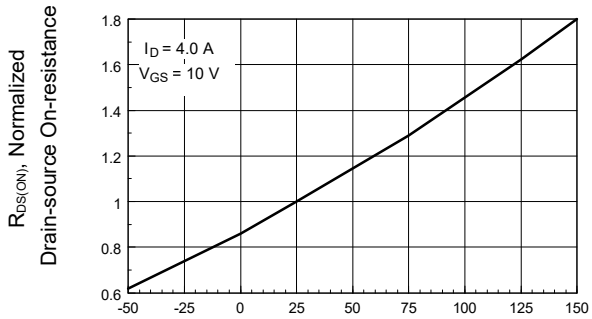


Figure 3: On-Resistance Variation with Temperature

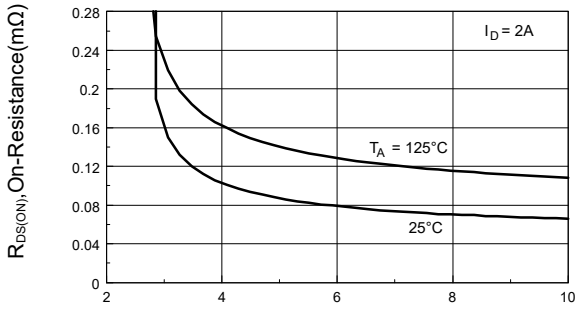


Figure 4: On-Resistance Variation with Gate-to-Source Voltage

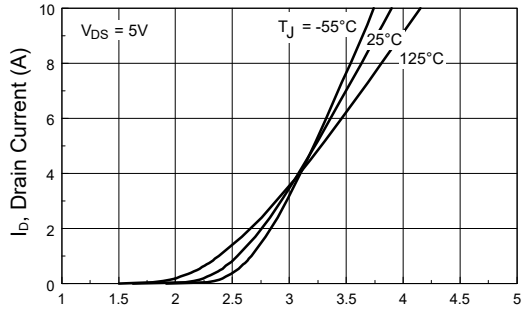


Figure 5: Transfer Characteristics

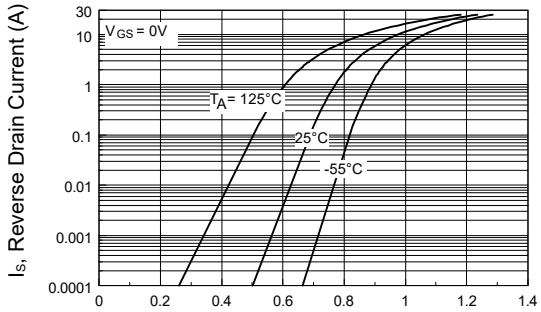


Figure 6: . Body Diode Forward Voltage Variation with Source Currentand Temperature

7.2Typical characteristic

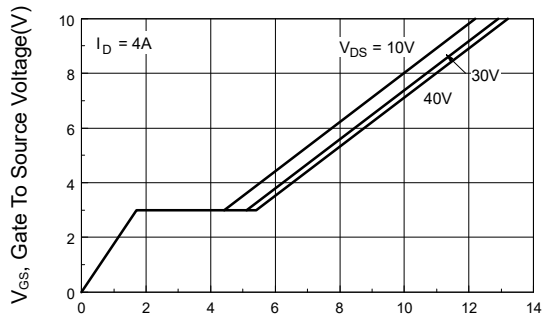


Figure 7: Gate Charge Characteristics

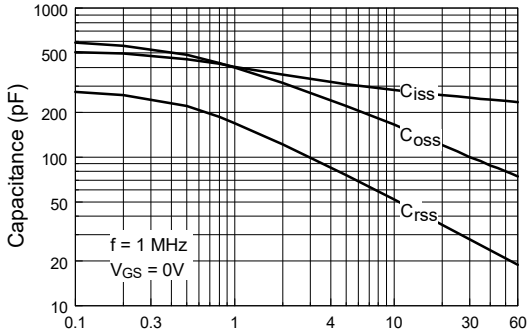


Figure 8: Capacitance Characteristics

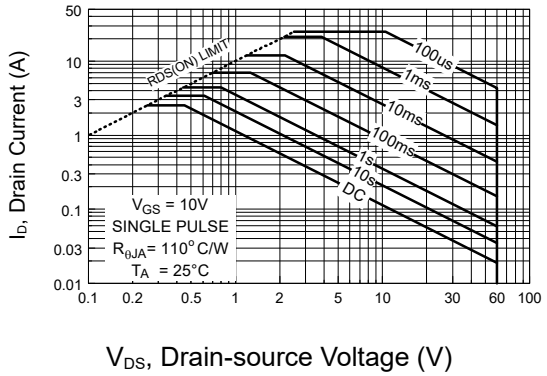


Figure 9: Maximum Safe Operating Area

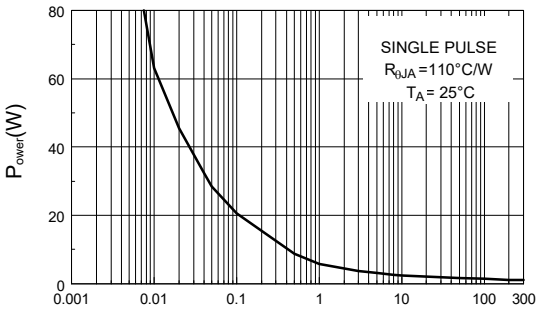


Figure 10: Single Pulse Maximum Power Dissipation

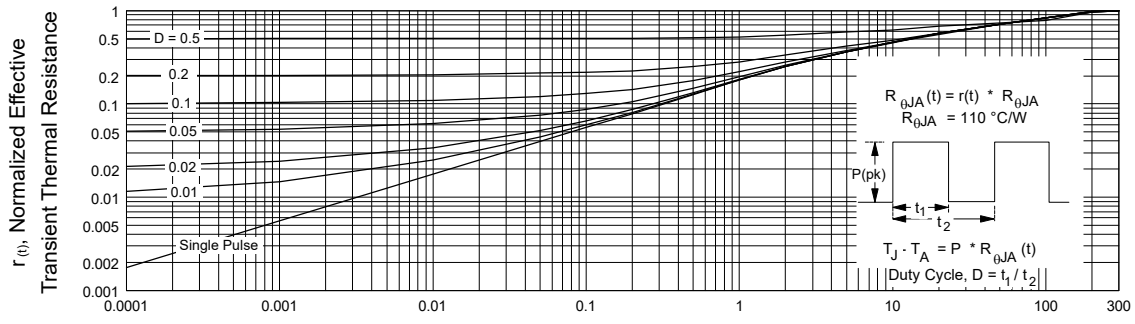
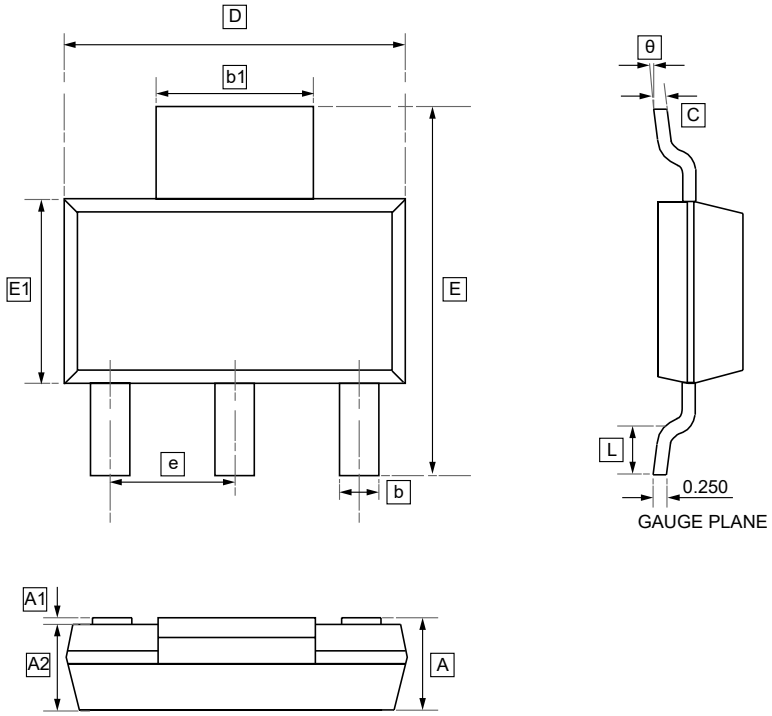


Figure 11: Transient Thermal Response Curve

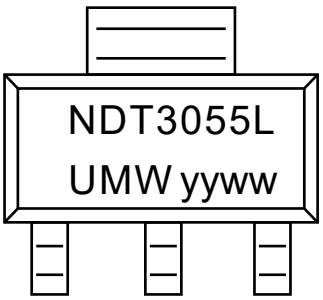
8.SOT-223 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	b1	c	D	E	E1	e	L	θ
Min	-	0.020	1.500	0.660	2.900	0.230	6.300	6.700	3.300	2.300	0.750	0°
Max	1.800	0.100	1.700	0.840	3.100	0.350	6.700	7.300	3.700	BSC	-	10°

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW NDT3055L	SOT-223	2500	Tape and reel

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