1048,576 WORD × 4 BIT DYNAMIC RAM

PRELIMINARY

DESCRIPTION

The TC514402AP/AJ/ASJ/AZ is the new generation dynamic RAM organized 1,048,576 words by 4 bits. The TC514402AP/AJ/ASJ/AZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514402AP/AJ/ASJ/AZ to be packaged in a standard 20 pin plastic DIP, 26/20 pin plastic SOJ (300/350mil) and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performace logic families such as Schottky TTL.

FEATURES

- 1,048,576 word by 4 bit organization
- Fast access time and cycle time

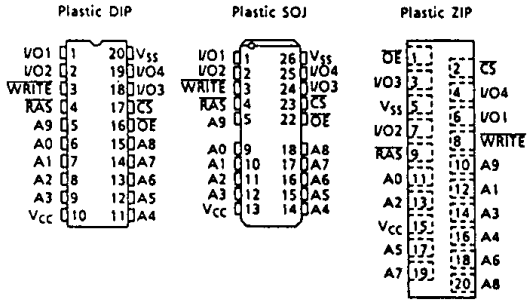
	TC514402AP/AJ/ASJ/AZ-70/-80/-10		
t_{RAC} $\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA} Column Address Access Time	35ns	40ns	50ns
t_{CAC} $\overline{CS}$ Access Time	20ns	20ns	25ns
t_{RC} Cycle Time	130ns	150ns	180ns
t_{SC} Static Column Mode Cycle Time	40ns	45ns	55ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  - 550mW MAX. Operating (TC514402AP/AJ/ASJ/AZ-70)
  - 468mW MAX. Operating (TC514402AP/AJ/ASJ/AZ-80)
  - 413mW MAX. Operating (TC514402AP/AJ/ASJ/AZ-10)
  - 5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Static Column Mode and Test Mode capability
- All inputs and outputs TTL Compatible
- 1024 refresh cycles/16ms
- Package
  - TC514402AP : DIP20-P-300C
  - TC514402AJ : SOJ26-P-350
  - TC514402ASJ : SOJ26-P-300A
  - TC514402AZ : ZIP20-P-400A

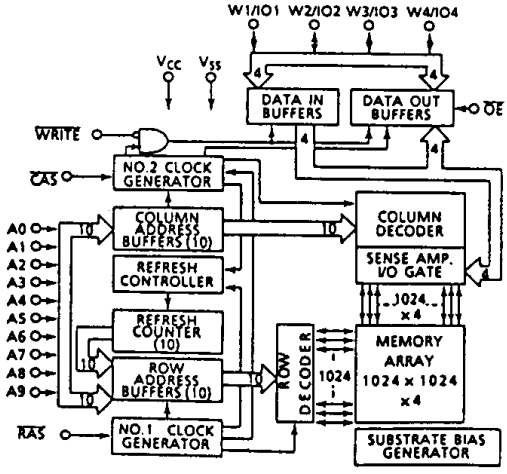
PIN NAMES

A0~A9	Address Inputs	$\overline{OE}$	Output Enable
$\overline{RAS}$	Row Address Strobe	I/O1~I/O4	Data Input/Output
$\overline{CS}$	Chip Select	V_{CC}	Power (+5V)
$\overline{WRITE}$	Read/Write Input	V_{SS}	Ground

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1~7	V	1
Output Voltage	V_{OUT}	-1~7	V	1
Power Supply Voltage	V_{CC}	-1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	-55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC514402AP/AJ/ASJ/AZ-70	–	100	mA	3, 4 5
		TC514402AP/AJ/ASJ/AZ-80	–	85		
		TC514402AP/AJ/ASJ/AZ-10	–	75		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC514402AP/AJ/ASJ/AZ-70	–	100	mA	3, 5
		TC514402AP/AJ/ASJ/AZ-80	–	85		
		TC514402AP/AJ/ASJ/AZ-10	–	75		
I_{CC4}	STATIC COLUMN MODE CURRENT Average Power Supply Current, STATIC COLUMN Mode ($\overline{RAS}$ = $\overline{CS}$ = V_{IL}, Address Cycling: t_{SC} = t_{SC} MIN.)	TC514402AP/AJ/ASJ/AZ-70	–	85	mA	3, 4 5
		TC514402AP/AJ/ASJ/AZ-80	–	75		
		TC514402AP/AJ/ASJ/AZ-10	–	70		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CS}$ = V_{CC} – 0.2V)		–	1	mA	
I_{CC6}	$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC514402AP/AJ/ASJ/AZ-70	–	100	mA	3, 5
		TC514402AP/AJ/ASJ/AZ-80	–	85		
		TC514402AP/AJ/ASJ/AZ-10	–	75		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins Not Under Test = 0V)		– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514402AP/ AJ/ASJ/AZ-70		TC514402AP/ AJ/ASJ/AZ-80		TC514402AP/ AJ/ASJ/AZ-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	-	150	-	180	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	185	-	205	-	245	-	ns	
t_{SC}	Static Column Mode Cycle Time	40	-	45	-	55	-	ns	
t_{SRMW}	Static Column Mode Read-Modify-Write Cycle Time	100	-	110	-	135	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	70	-	80	-	100	ns	9,14 15
t_{CAC}	Access Time from $\overline{CS}$	-	20	-	20	-	25	ns	9,14
t_{AA}	Access Time from Column Address	-	35	-	40	-	50	ns	9,15
t_{ALW}	Access Time from Last Write	-	65	-	75	-	95	ns	9,16
t_{CLZ}	$\overline{CS}$ to output in Low-Z	0	-	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	10
t_{AOH}	Output Data Hold Time from Column Addres	5	-	5	-	5	-	ns	
t_{OW}	Output Data Enable Time from $\overline{WRITE}$	-	20	-	20	-	30	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	50	-	60	-	70	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	70	200,000	80	200,000	100	200,000	ns	
t_{RSH}	$\overline{CS}$ to $\overline{RAS}$ Hold Time	20	-	20	-	25	-	ns	
t_{CSH}	$\overline{RAS}$ to $\overline{CS}$ Hold Time	70	-	80	-	100	-	ns	
t_{CS}	$\overline{CS}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	20	200,000	20	200,000	25	200,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CS}$ Delay Time	20	50	20	60	25	75	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	15
t_{CRP}	$\overline{CS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	10	-	ns	
t_{CP}	$\overline{CS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	20	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$ (READ CYCLE)	85	-	95	-	115	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	50	-	ns	
t_{AH}	Column Address Hold Time referenced to $\overline{RAS}$ Rise	5	-	5	-	10	-	ns	17

SYMBOL	PARAMETER	TC514402AP/ AJ/ASJ/AZ-70		TC514402AP/ AJ/ASJ/AZ-80		TC514402AP/ AJ/ASJ/AZ-10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{LWAD}	Last Write to Column Address Delay Time	20	30	20	35	25	45	ns	16
t_{AHLW}	Last Write to Column Address Hold Time	65	–	75	–	95	–	ns	
t_{RCS}	Read Command Set-up Time referenced to $\overline{CS}$	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time referenced to $\overline{CS}$	0	–	0	–	0	–	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time (Output Data Disable)	15	–	15	–	20	–	ns	13
t_{WP}	Write Command Pulse Width	15	–	15	–	20	–	ns	
t_{WI}	Write Command Inactive Time	10	–	10	–	10	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CS}$ Lead Time	20	–	20	–	25	–	ns	
t_{DS}	Data-In Set-Up Time	0	–	0	–	0	–	ns	12
t_{DH}	Data-In Hold Time	15	–	15	–	20	–	ns	12
t_{REF}	Refresh Period	–	16	–	16	–	16	ms	
t_{WCS}	Write Command Set-UP Time (Output Data Disable)	0	–	0	–	0	–	ns	13
t_{CWD}	$\overline{CS}$ to $\overline{WRITE}$ Delay Time (READ-MODIFY-WRITE CYCLE)	50	–	50	–	60	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time (READ-MODIFY-WRITE Cycle)	100	–	110	–	135	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	65	–	70	–	85	–	ns	13
t_{CSR}	$\overline{CS}$ Set-Up Time($\overline{CS}$ before $\overline{RAS}$)	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{CS}$ Hold Time($\overline{CS}$ before $\overline{RAS}$)	15	–	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CS}$ Precharge Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	40	–	50	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	10	–	20	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	20	–	20	–	25	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	–	20	–	25	–	ns	
t_{OEZ}	Output Buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	0	20	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	20	–	20	–	25	–	ns	

SYMBOL	PARAMETER	TC514402AP/ AJ/ASJ/AZ-70		TC514402AP/ AJ/ASJ/AZ-80		TC514402AP/ AJ/ASJ/AZ-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WTS}	Write Command Set-Up Time	10	–	10	–	10	–	ns	
t_{WTH}	Write Command Hold Time	10	–	10	–	10	–	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time	10	–	10	–	10	–	ns	
t_{WRH}	WRITE to RAS Hold Time	10	–	10	–	10	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN THE TEST MODE (V_{CC} = 5V ± 10%, Ta = 0~70°c) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514402AP/AJ/ASJ/AZ-70		TC514402AP/AJ/ASJ/AZ-80		TC514402AP/AJ/ASJ/AZ-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	135	–	155	–	185	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	190	–	210	–	250	–	ns	
t_{SC}	Static Column Mode Cycle Time	45	–	50	–	60	–	ns	
t_{SRMW}	Static Column Mode Read-Modify-Write Cycle Time	105	–	115	–	140	–	ns	
t_{RAC}	Access Time from $\overline{CS}$	–	75	–	85	–	105	ns	9,14 15
t_{CAC}	Access Time from $\overline{CS}$	–	25	–	25	–	30	ns	9,14
t_{AA}	Access Time from Column Address	–	40	–	45	–	50	ns	9,15
t_{ALW}	Access Time from Last Write	–	70	–	80	–	100	ns	9,16
t_{RAS}	$\overline{RAS}$ Pulse Width	75	10,000	85	10,000	105	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	75	200,000	85	200,000	105	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	–	25	–	30	–	ns	
t_{CSH}	$\overline{CS}$ Hold Time	75	–	85	–	105	–	ns	
t_{CS}	$\overline{CS}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	25	200,000	25	200,000	30	200,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	–	45	–	55	–	ns	
t_{CWD}	$\overline{CS}$ to $\overline{WRITE}$ Delay Time	60	–	60	–	70	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Dalay Time	105	–	115	–	140	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	70	–	75	–	90	–	ns	13
t_{OEA}	$\overline{OE}$ Access Time	–	25	–	25	–	30	ns	
t_{OED}	$\overline{OE}$ to Data Delay	25	–	25	–	30	–	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	25	–	25	–	30	–	ns	

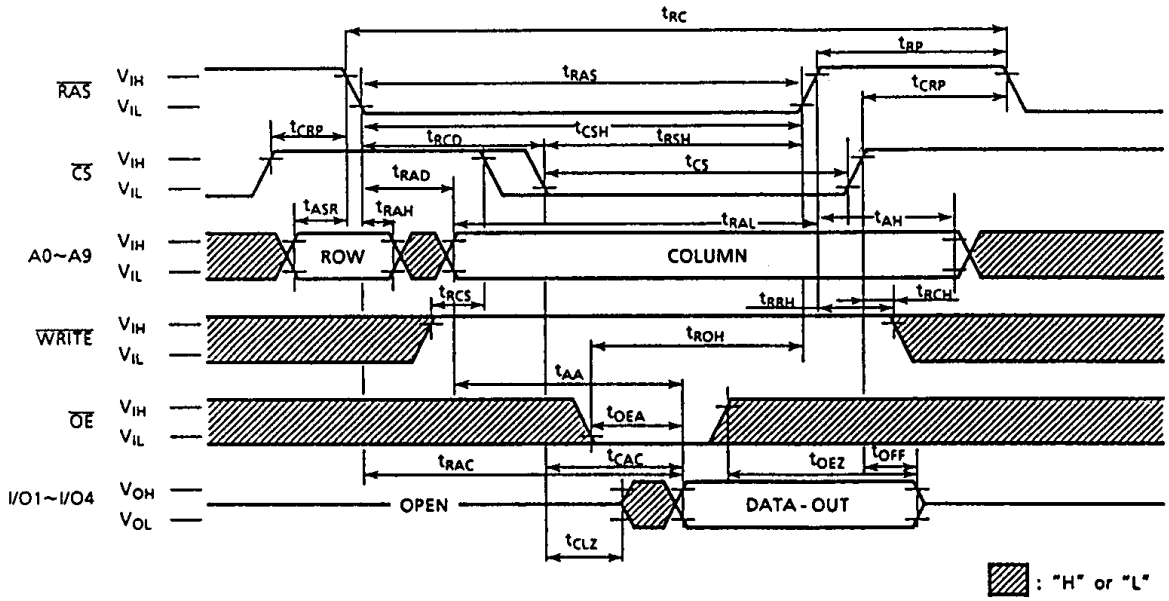
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A9)	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WRITE}$, $\overline{OE}$)	–	7	pF
C_O	Input/Output Capacitance (I/O1~I/O4)	–	7	pF

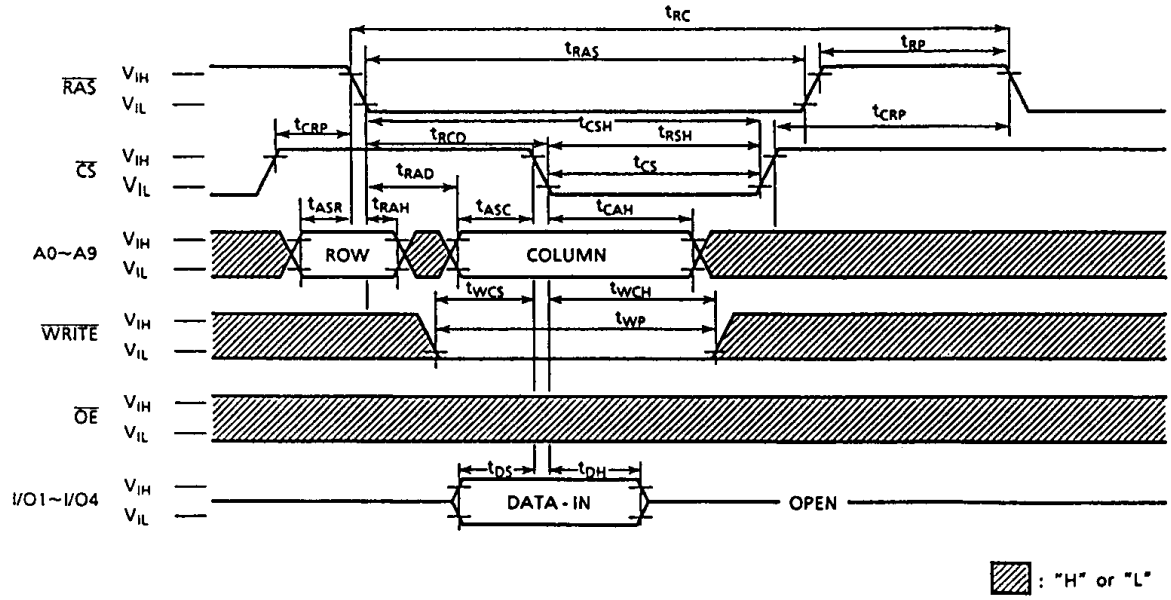
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS}=V_{IL}$ and $\overline{CS}=V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ refresh cycles are required.
7. AC measurements assume $t_T=5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.) and $t_{AWD} \geqq t_{AWD}$ (min.) the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.
16. Operation within the t_{LWAD} (max.) limit insures that t_{ALW} (max.) can be met.
    t_{LWAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{LWAD} (max.) limit, then access time is controlled by t_{AA}.
17. t_{AH} is the condition to latch column address ewhen $\overline{RAS}$ has rised up.

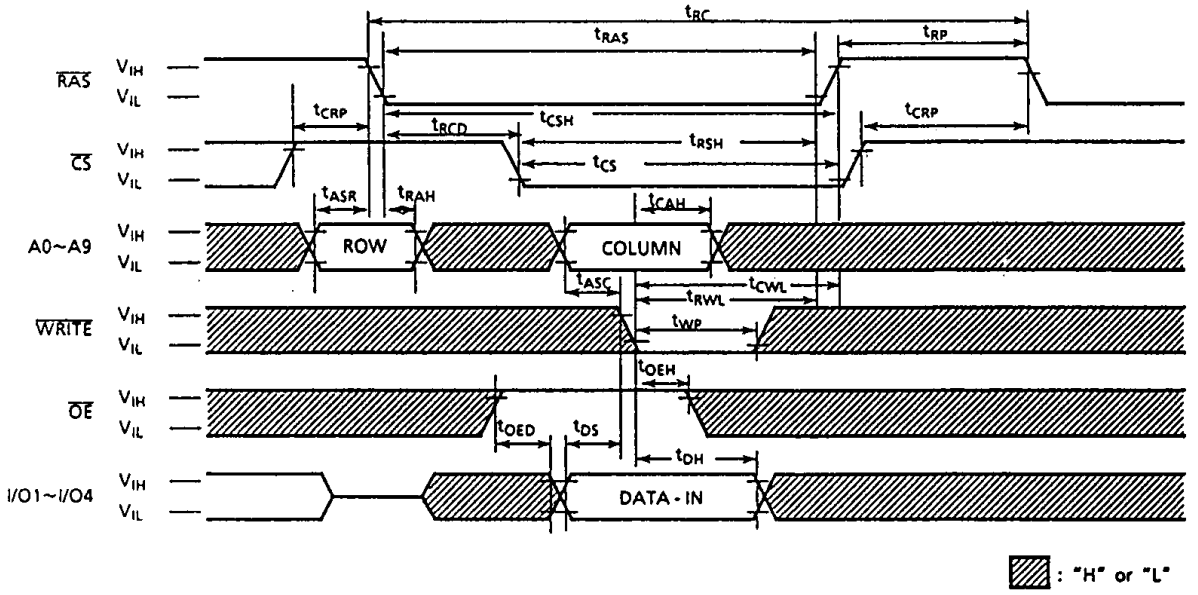
READ CYCLE



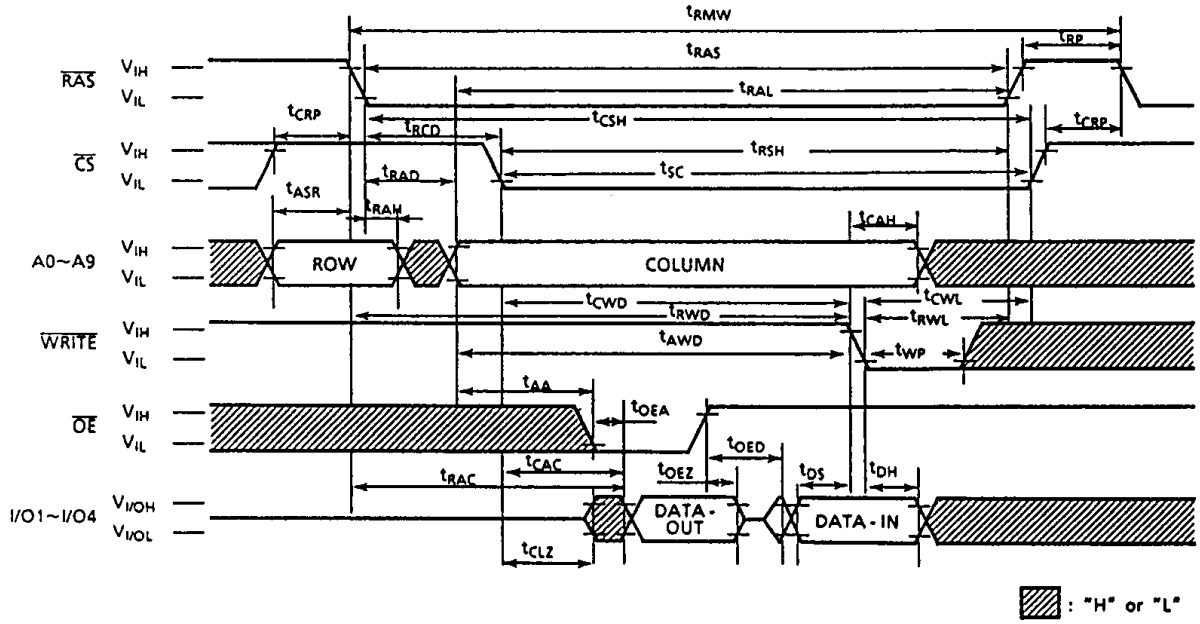
WRITE CYCLE (EARLY WRITE)



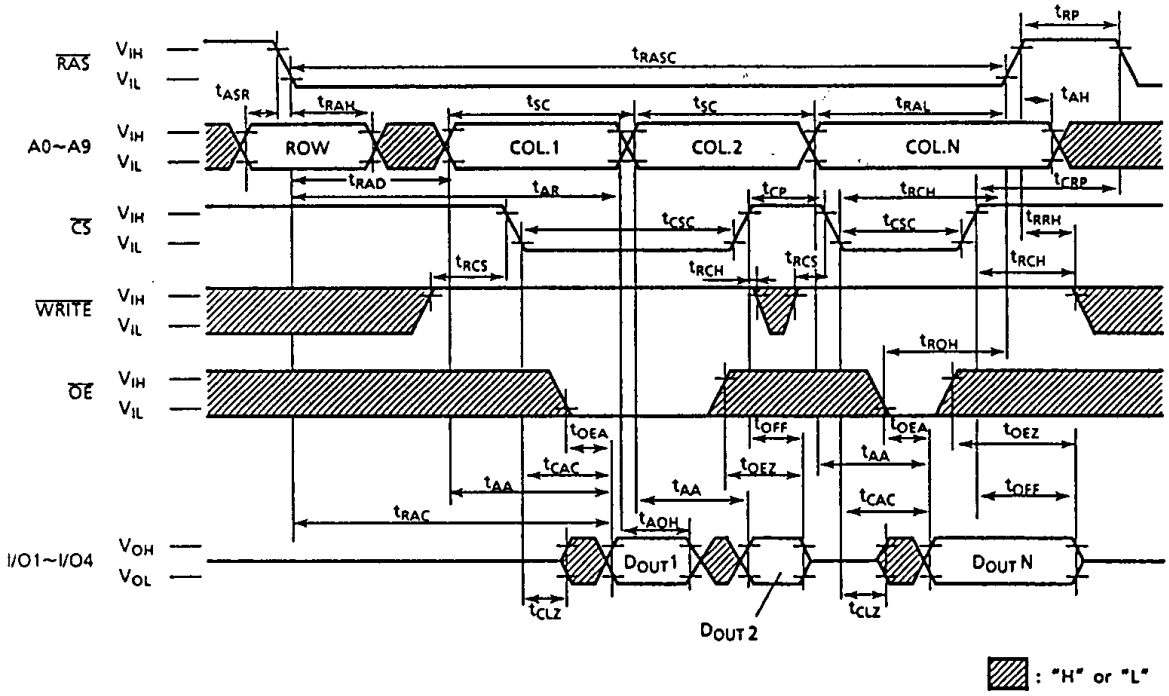
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



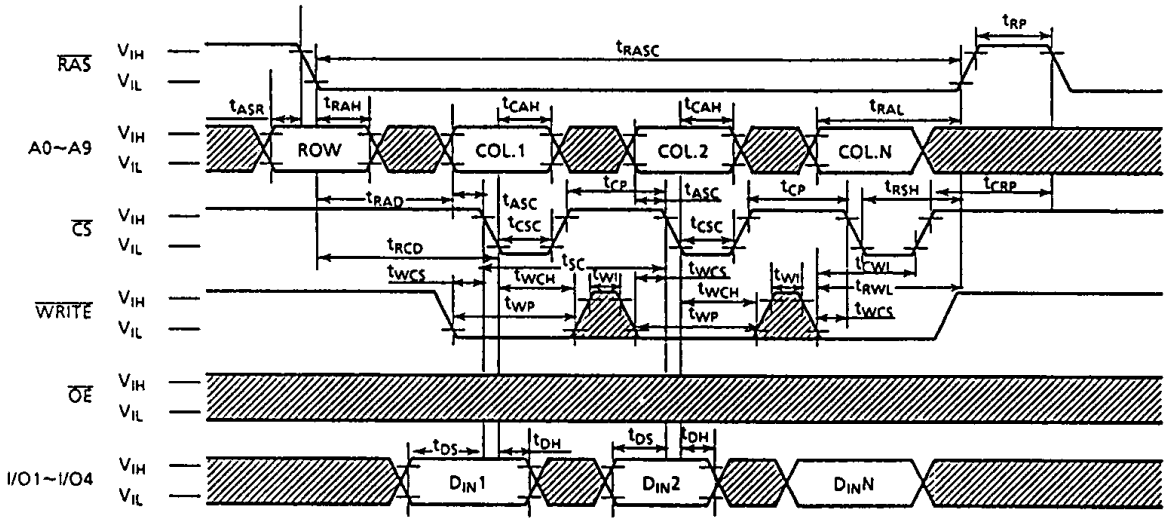
READ - MODIFY - WRITE CYCLE



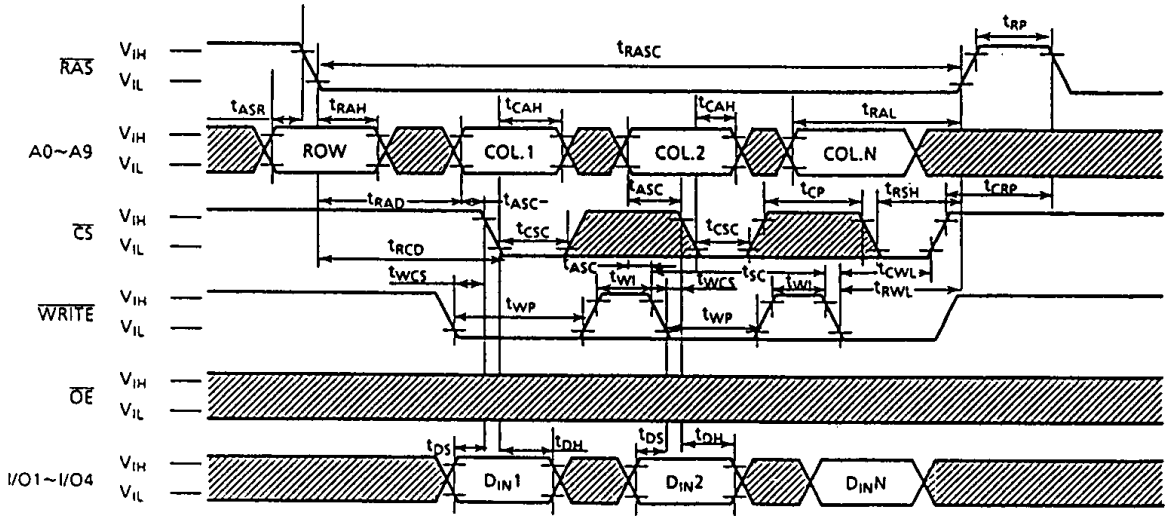
STATIC COLUMN MODE READ CYCLE



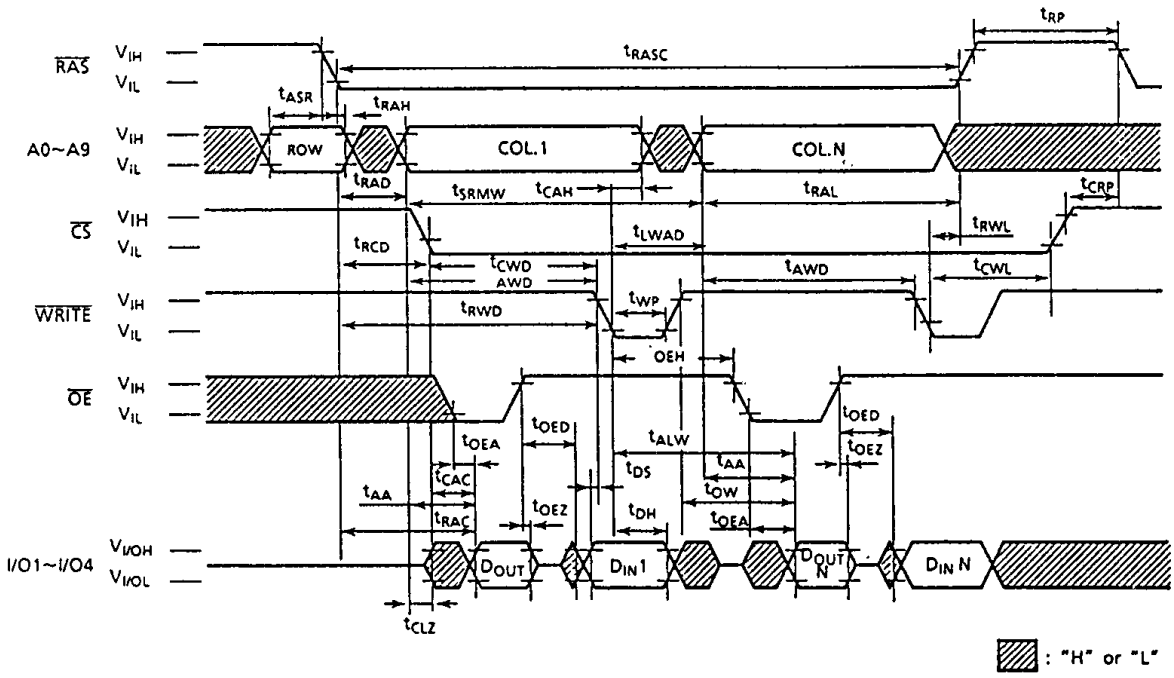
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



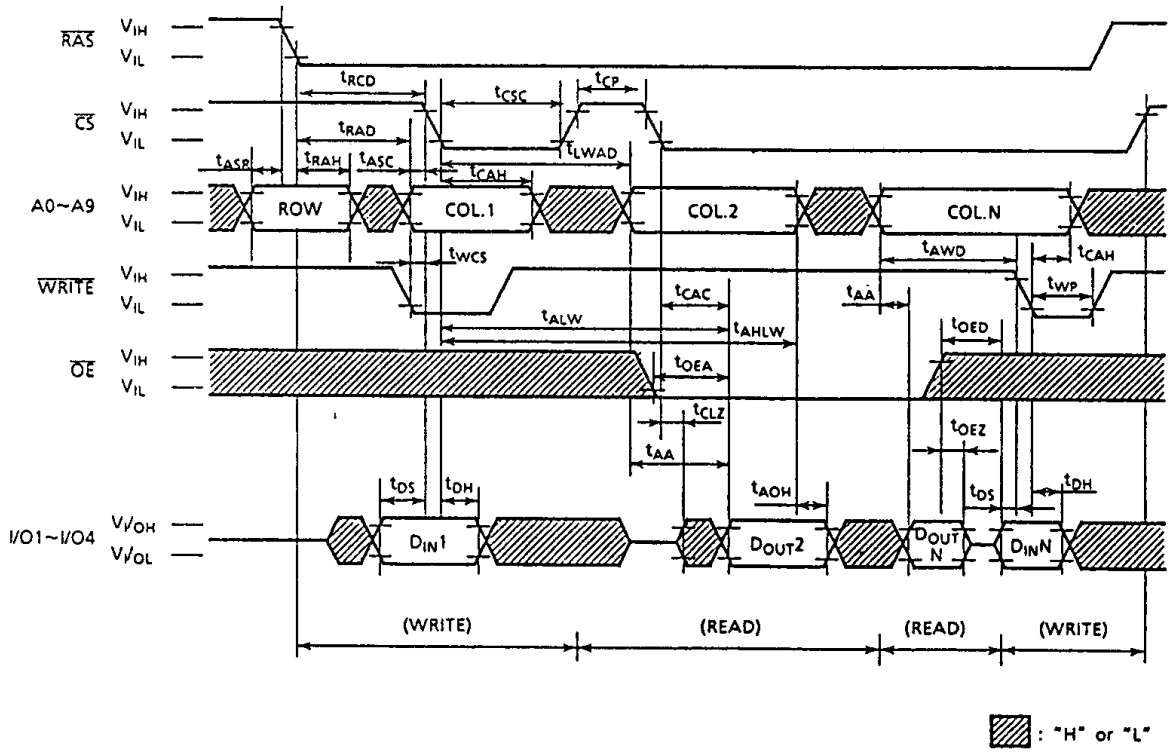
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



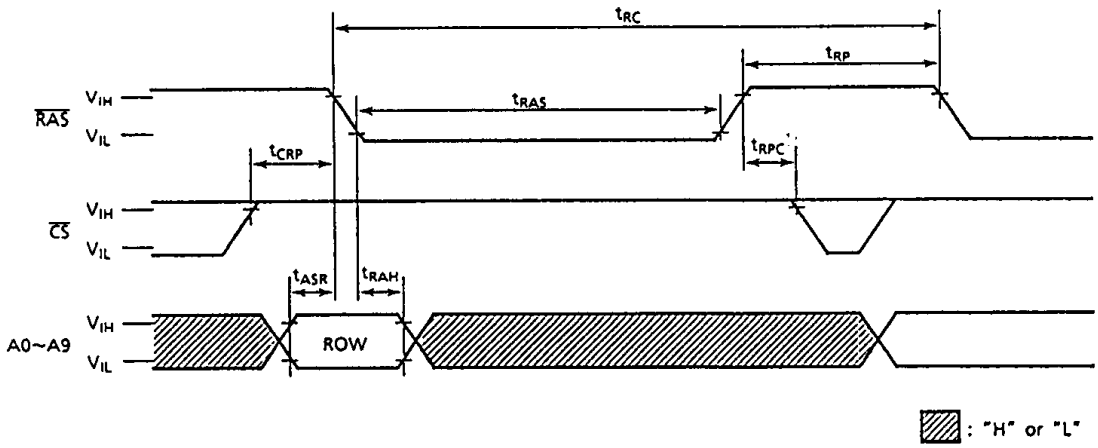
STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE



STATIC COLUMN MODE READ/WRITE MIXED CYCLE

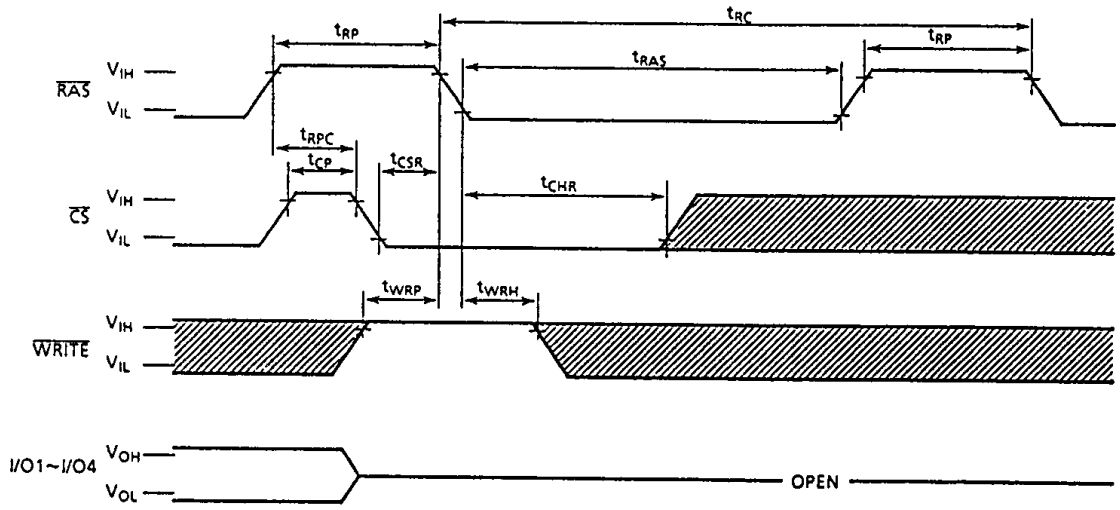


$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$, $\overline{OE}$ = "H" or "L"

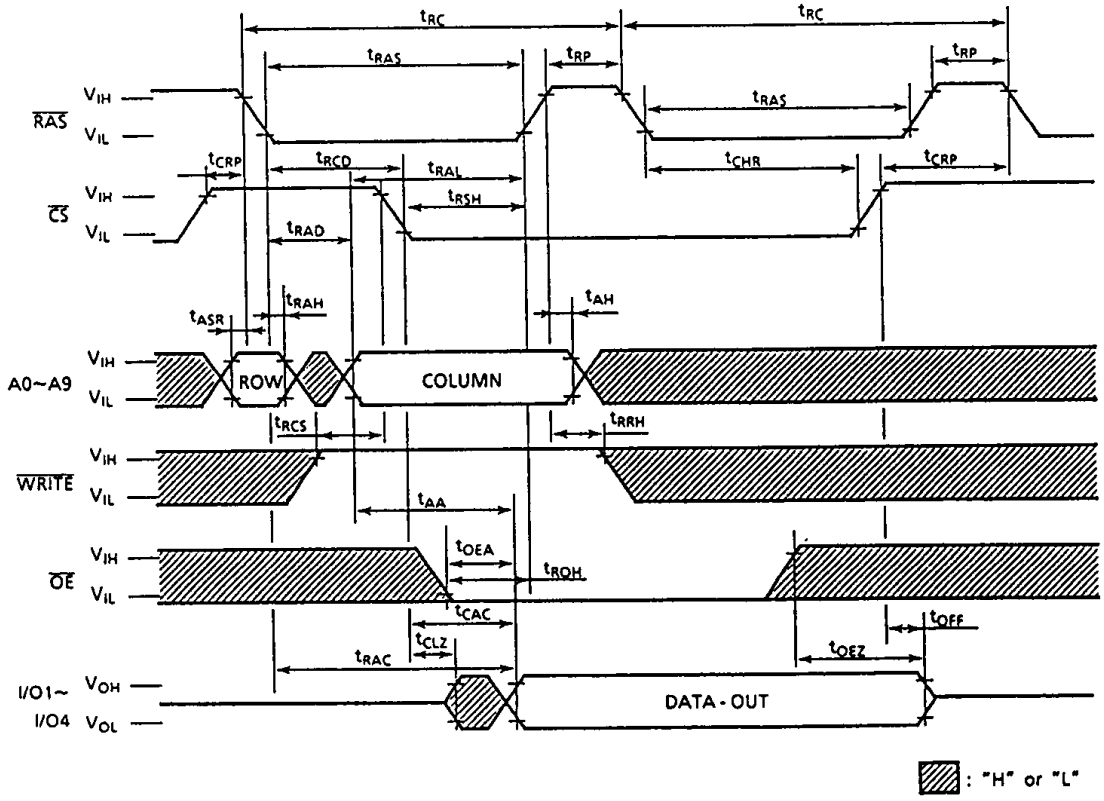
$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



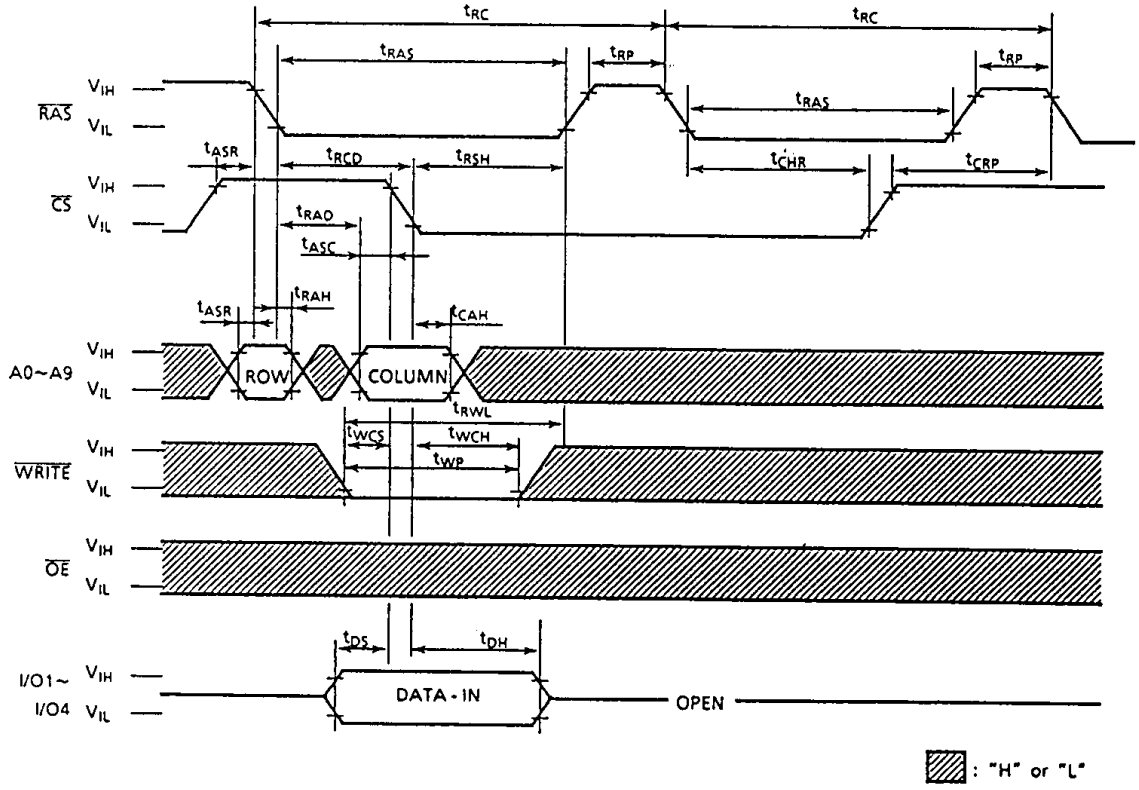
Note: $\overline{OE}$, A0~A9 = "H" or "L"

▨ : "H" or "L"

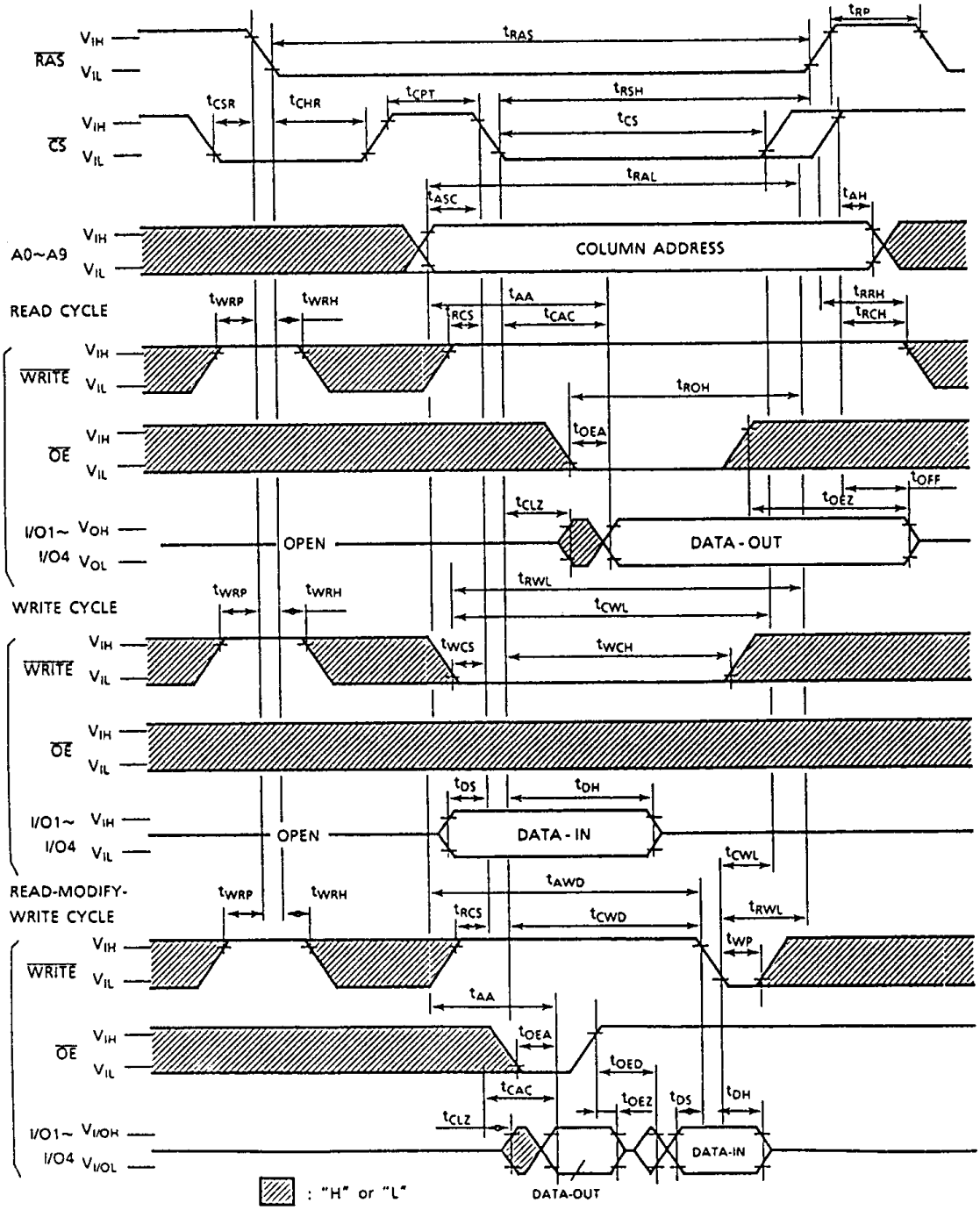
HIDDEN REFRESH CYCLE (READ)



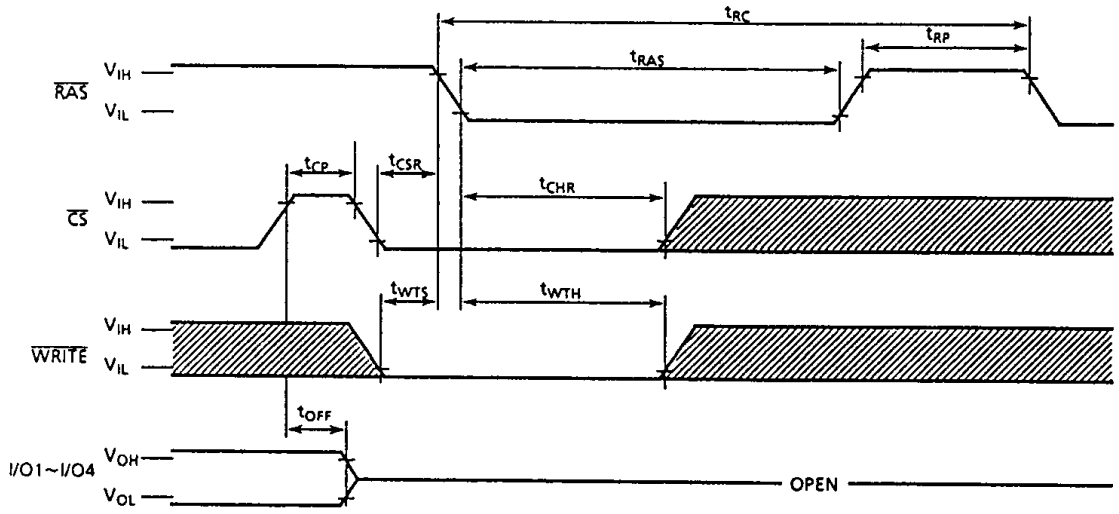
HIDDEN REFRESH CYCLE (WRITE)



$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



WRITE, $\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: $\overline{OE}$, A0~A9 = "H" or "L"

▨ : "H" or "L"

TEST MODE

The TC514402AP/AJ/ASJ/AZ is the RAM organized 1,048,576 words by 4 bits, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A0C is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". Fig. 1 shows the block diagram of TC514402AP/AJ/ASJ/AZ. In "Test Mode", the 1M×4 DRAM can be tested as if it were a 512K×4 DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" puts the device into "Test Mode". And "$\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle "or "$\overline{\text{RAS}}$ Only Refresh Cycle" put it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/2 in cace of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

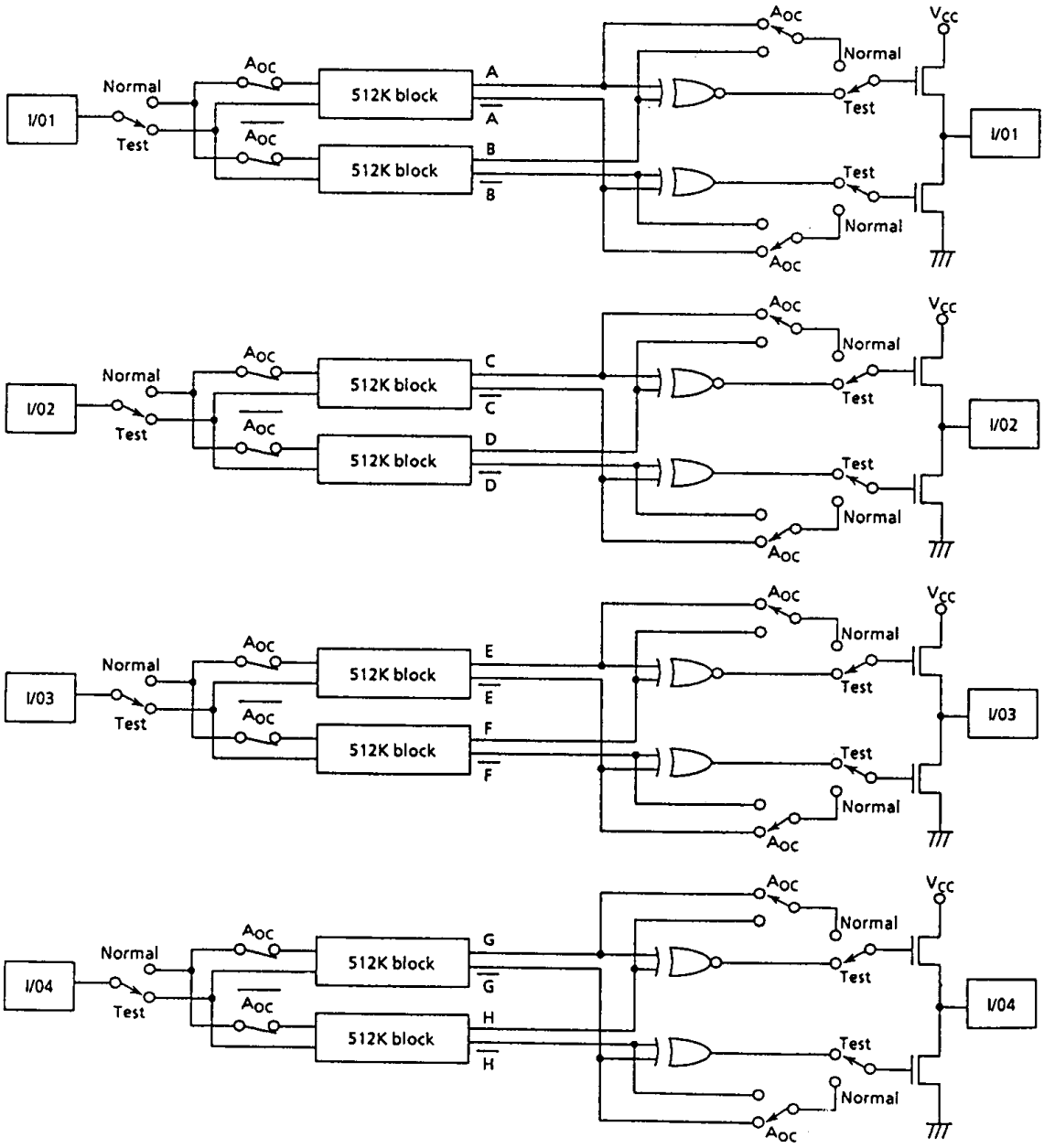


Fig. 1