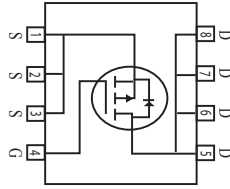


Surface Mount P-Channel Enhancement Mode MOSFET

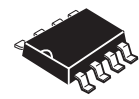
(Pb) Lead(Pb)-Free

Features:

- *Super high dense cell design for low $R_{DS(ON)}$
- $R_{DS(ON)} < 55 \text{ m}\Omega @ V_{GS} = -10\text{V}$
- $R_{DS(ON)} < 85 \text{ m}\Omega @ V_{GS} = -4.5\text{V}$
- *Rugged and Reliable
- *SO-8 Package



DRAIN CURRENT
-4.8 AMPERS
DRAIN SOURCE VOLTAGE
-30 VOLTAGE



1
SO-8

Maximum Ratings (TA=25°C Unless Otherwise Specified)

Rating	Symbol	Value	Unite
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($T_J = 125^\circ\text{C}$) ⁽¹⁾	I_D	-4.8	A
Pulsed Drain Current ⁽²⁾	I_{DM}	-24	A
Drain-Source Diode Forward Current (1)	I_S	-1.7	A
Power Dissipation (1)	P_D	2.5	W
Maximax Junction-to-Ambient	$R_{\theta JA}$	50	$^\circ\text{C/W}$
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Device Marking

WT9435M=STM9435

Electrical Characteristics ($T_A=25^\circ\text{C}$ Unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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Static (2)

Drain-Source Breakdown Voltage $V_{GS}=0V, I_D=-250\ \mu\text{A}$	$V_{(BR)DSS}$	-30	-	-	V
Gate-Source Threshold Voltage $V_{DS}=V_{GS}, I_D=-250\ \mu\text{A}$	$V_{GS(th)}$	-1	-1.5	-2.5	V
Gate-Source Leakage Current $V_{DS}=0V, V_{GS}=\pm 20V$	I_{GSS}	-	-	± 100	nA
Zero Gate Voltage Drain Current $V_{DS}=-24V, V_{GS}=0V$	I_{DSS}	-	-	-1	μA
Drain-Source On-Resistance $V_{GS}=-10V, I_D=-5.3A$ $V_{GS}=-4.5V, I_D=-4.2A$	$r_{DS(on)}$	- -	45 75	55 85	$\text{m}\Omega$
On-State Drain Current $V_{DS}=-5V, V_{GS}=-10A$	$I_{D(on)}$	-20	-	-	A
Forward Transconductance $V_{DS}=-5V, I_D=-5.3A$	g_{fs}	-	5	-	S

Dynamic (3)

Input Capacitance $V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	C_{iss}	-	582	-	PF
Output Capacitance $V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	C_{oss}	-	125	-	
Reverse Transfer Capacitance $V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	C_{rss}	-	86	-	

Switching (3)

Turn-On Delay Time $V_{GEN}=-10V, V_{DD}=-15V, I_D=-1A, R_L=15\ \Omega, R_{GEN}=6\ \Omega$	$t_{d(on)}$	-	9	-	nS
Rise Time $V_{GEN}=-10V, V_{DD}=-15V, I_D=-1A, R_L=15\ \Omega, R_{GEN}=6\ \Omega$	t_r	-	10	-	nS
Turn-Off Time $V_{GEN}=-10V, V_{DD}=-15V, I_D=-1A, R_L=15\ \Omega, R_{GEN}=6\ \Omega$	$t_{d(off)}$	-	37	-	nS
Fall Time $V_{GEN}=-10V, V_{DD}=-15V, I_D=-1A, R_L=15\ \Omega, R_{GEN}=6\ \Omega$	t_f	-	23	-	nS
Total Gate Charge $V_{DS}=-15V, I_D=-5.3A, V_{GS}=-10V$ $V_{DS}=-15V, I_D=-5.3A, V_{GS}=-4.5V$	Q_g	- -	11.7 5.7	- -	nc
Gate-Source Charge $V_{DS}=-15V, I_D=-5.3A, V_{GS}=-10V$	Q_{gs}	-	2.1	-	nc
Gate-Drain Charge $V_{DS}=-15V, I_D=-5.3A, V_{GS}=-10V$	Q_{gd}	-	2.9	-	nc
Drain-Source Diode Forward Voltage $V_{GS}=0V, I_S=-1.7A$	V_{SD}	-	-0.84	-1.2	V

Note: 1. Surface Mounted on FR4 Board $t \leq 10\text{sec}$.

2. Pulse Test : $PW \leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

3. Guaranteed by Design, not Subject to Production Testing.

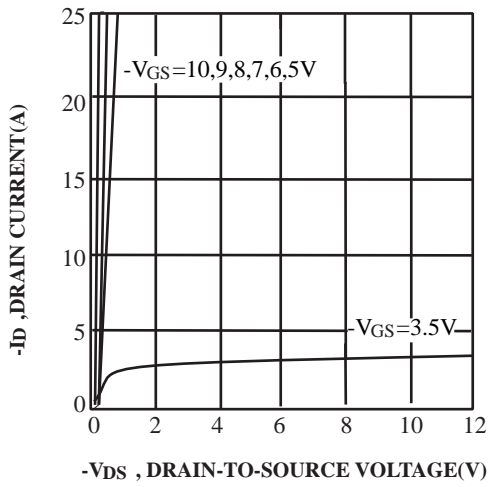


FIG.1. Output Characteristics

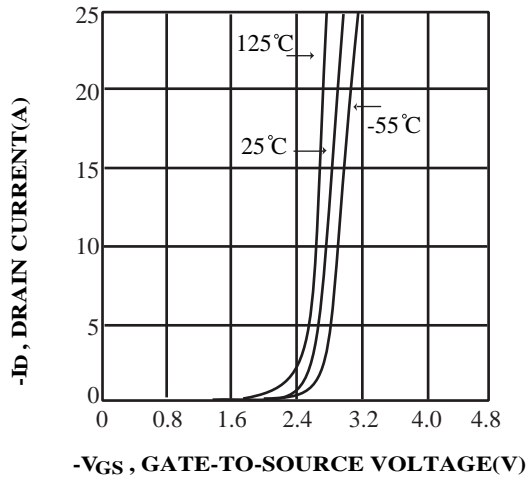


FIG.2 Transfer Characteristics

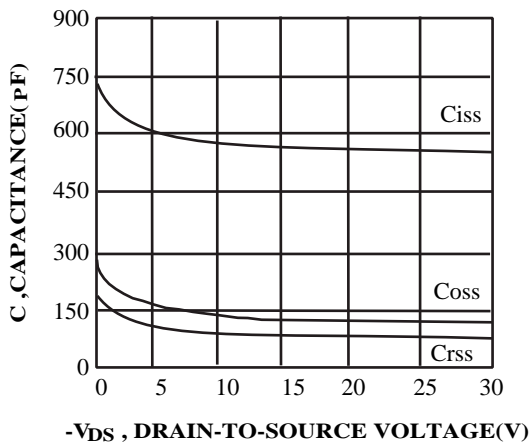


FIG.3 Capacitance

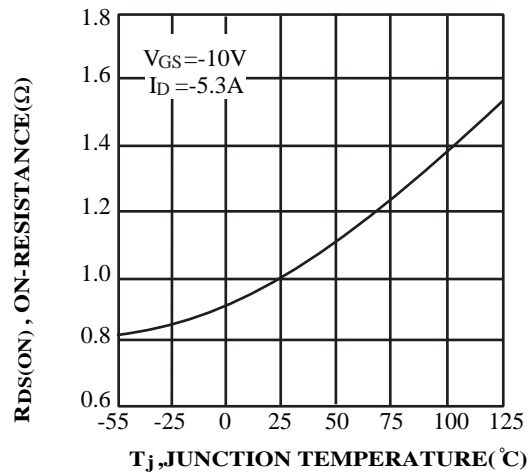


FIG.4 On-Resistance Variation with Drain Current and Temperature

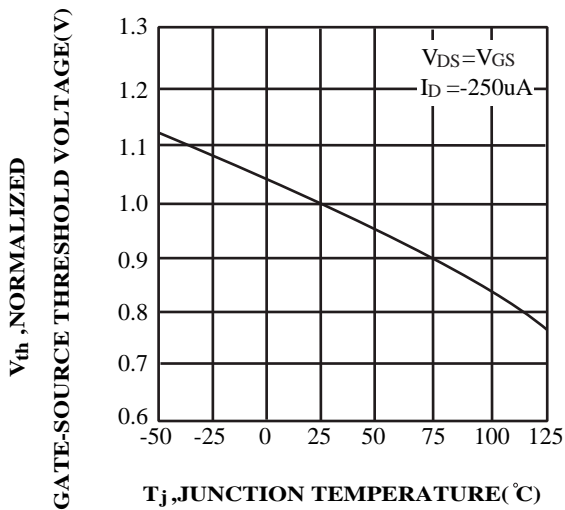


FIG.5 Gate Threshold Variation with Temperature

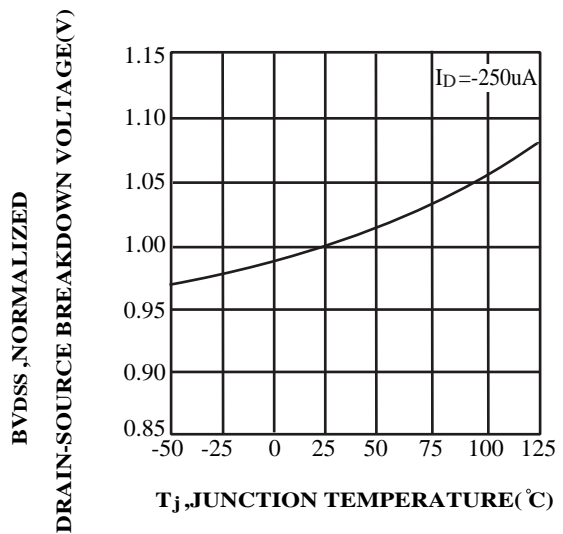
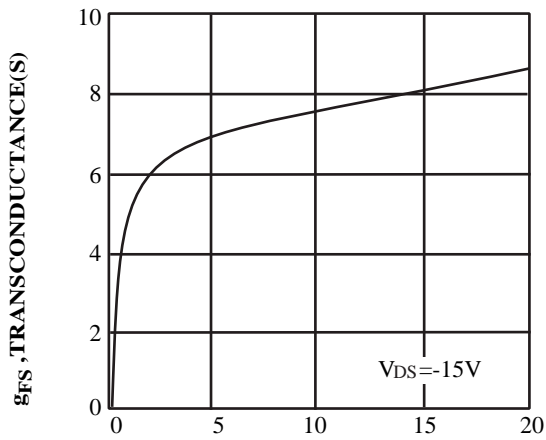
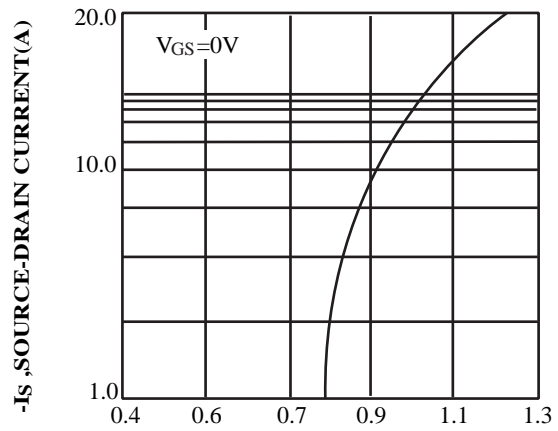


FIG.6 Breakdown Voltage Variation with Temperature



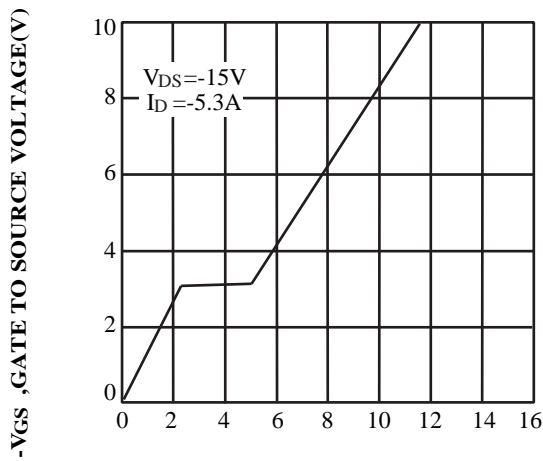
-IDS ,DRAIN-SOURCE CURRENT(A)

FIG.7 Transconductance Variation with Drain Current



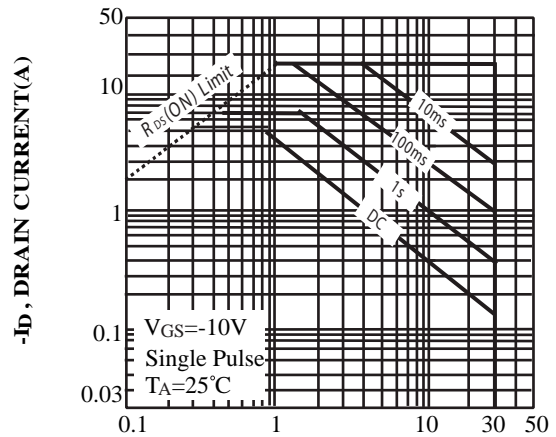
VSD ,BODY DIODE FORWARD VOLTAGE(V)

FIG.8 Body Diode Forward Voltage Variation with Source Current



Qg ,TOTAL GATE CHARGE(nC)

FIG.9 Gate Charge



-VDS ,DRAIN-SOURCE VOLTAGE(V)

FIG.10 Maximum Safe Operating Area

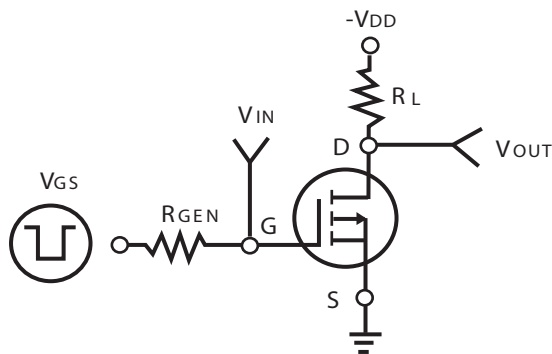


FIG.11 Switching Test Circuit

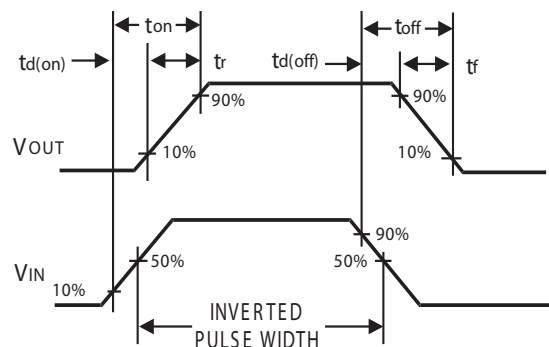


FIG.12 Switching Waveforms

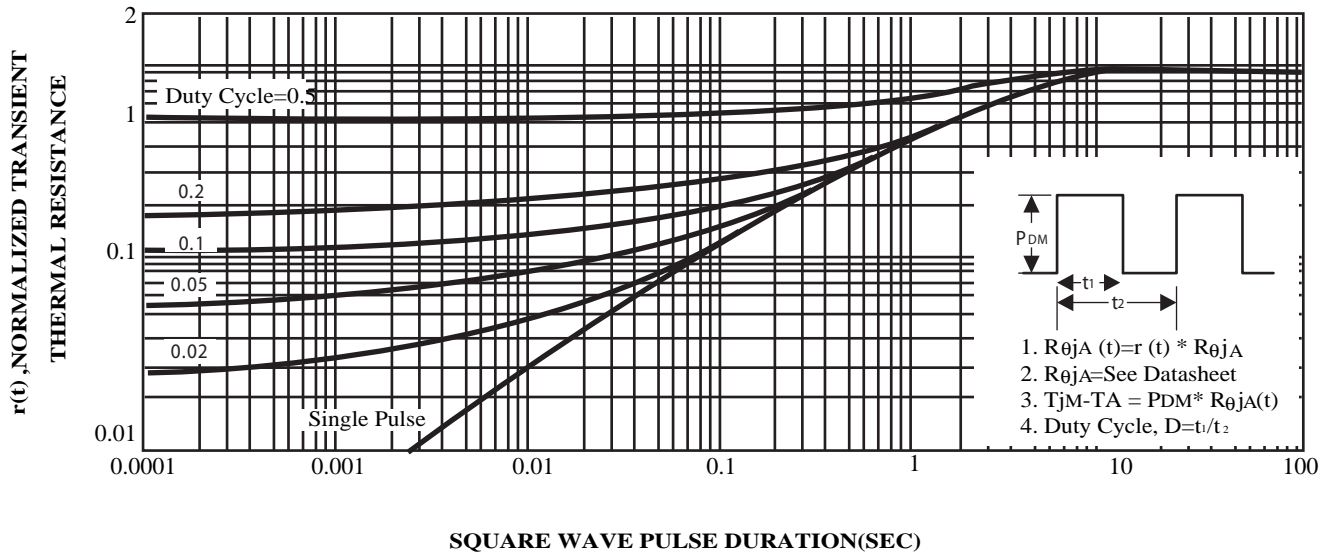
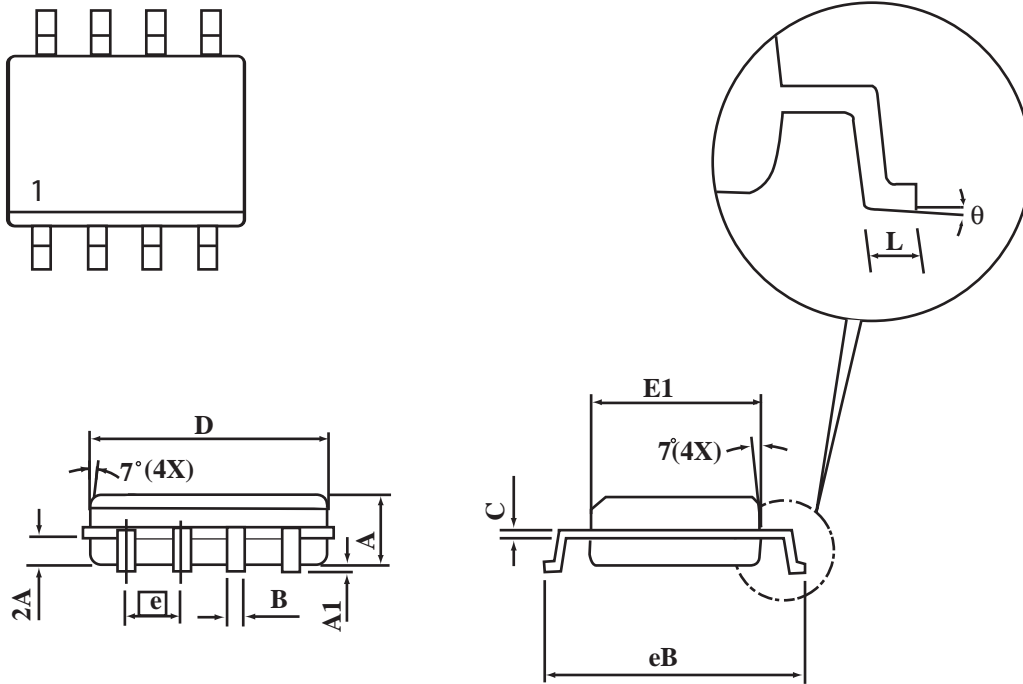


FIG.13 NORMALIZED THERMAL TRANSIENT IMPEDANCE CUREVE

SO-8 Package Outline Dimensions

Unit:mm



SYMBOLS	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.20
B	0.35	0.45
C	0.18	0.23
D	4.69	4.98
E1	3.56	4.06
eB	5.70	6.30
e	1.27 BSC	
L	0.60	0.80
θ	0°	8°