

CD40194B Types

CMOS 4-Bit Bidirectional Universal Shift Register

High-Voltage Types (20 Volt Rating)

■ CD40194B is a universal shift register featuring parallel inputs, parallel outputs SHIFT RIGHT and SHIFT LEFT serial inputs, and a direct overriding clear input. In the parallel-load mode (S0 and S1 are high), data is loaded into the associated flip-flop and appears at the output after the positive transition of the CLOCK input. During loading, serial data flow is inhibited. Shift right and shift left are accomplished synchronously on the positive clock edge with data entered at the SHIFT RIGHT and SHIFT LEFT serial inputs, respectively. Clocking of the register is inhibited when both mode control inputs are low. When low, the RESET input resets all stages and forces all outputs low.

The CD40194B types are supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
Voltages referenced to V _{SS} Terminal	-0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to V _{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT	±10mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T _A = -55°C to +100°C	500mW
For T _A = +100°C to +125°C	Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T _A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100mW
OPERATING-TEMPERATURE RANGE (T_A)	-55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg})	-65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max	+265°C

NOT RECOMMENDED FOR NEW DESIGNS

Features:

- Medium-speed: f_{CL} = 12 MHz (typ.) @ V_{DD} = 10 V
- Fully static operation
- Synchronous parallel or serial operation
- Asynchronous master reset
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Arithmetic unit bus registers
- Serial/parallel conversions
- General-purpose register for bus-organized systems
- General-purpose registers

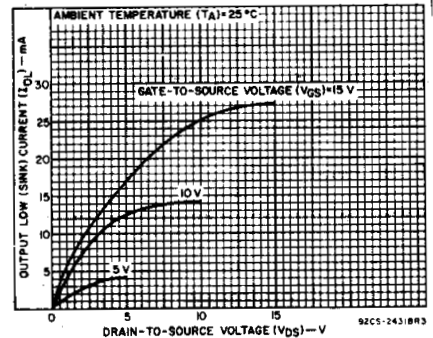
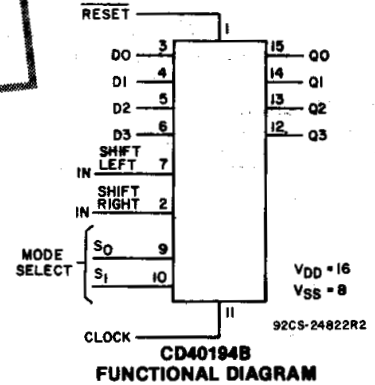


Fig. 1—Typical n-channel output low (sink) current characteristics.

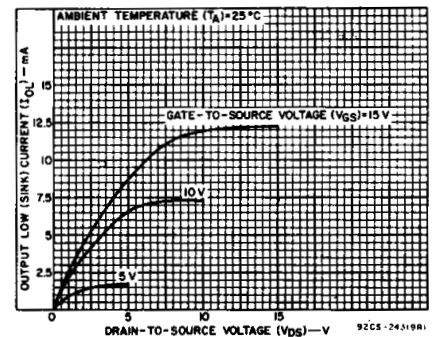


Fig. 2—Minimum n-channel output low (sink) current characteristics.

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RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	VDD (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For Package-Temperature Range)		3	18	V
Setup Time, D0, D3, SR _{IN} , SL _{IN} to clock SELECT 0, SELECT 1 to clock	5	100	—	ns
	10	70	—	
	15	50	—	
Hold Time, D0, D3, SR _{IN} , SL _{IN} to clock SELECT 0, SELECT 1 to clock	5	0	—	ns
	10	0	—	
	15	0	—	
Clock Pulse Width, t _w	5	180	—	ns
	10	80	—	
	15	50	—	
Clock Input Frequency f _{CL}	5	—	3	MHz
	10	—	6	
	15	—	8	
Clock Input Rise or Fall Time, t _{rCL} , t _{fCL}	5	1000	—	μs
	10	100	—	
	15	100	—	
Reset Pulse Width, t _{WR}	5	300	—	ns
	10	200	—	
	15	140	—	

CONTROL TRUTH TABLE FOR CD40194B SERIES

CLOCK	MODE SELECT		RESET	ACTION
	S ₀	S ₁		
X	0	0	1	No Change
	1	0	1	Shift Right (Q0 toward Q3)
	0	1	1	Shift Left (Q3 toward Q0)
	1	1	1	Parallel Load
X	X	X	0	Reset

1 = High level
 0 = Low level

X = Don't care
 ▲ = Level change

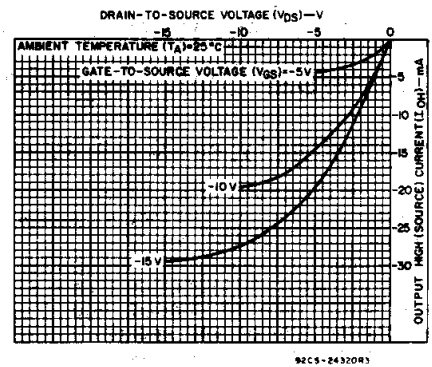


Fig. 3—Typical p-channel output high (source) current characteristics.

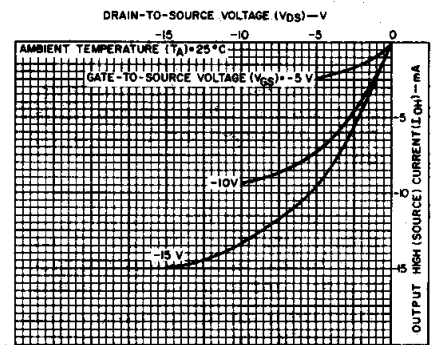


Fig. 4—Minimum p-channel output high (source) current characteristics.

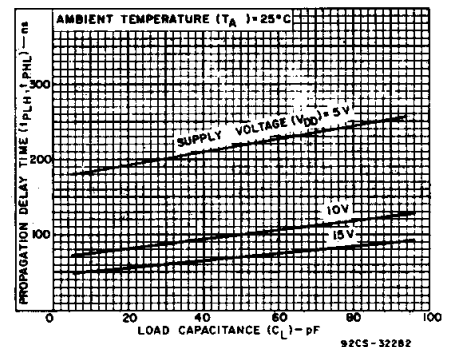


Fig. 5—Typical propagation delay time as a function of load capacitance, (CLOCK to Q).

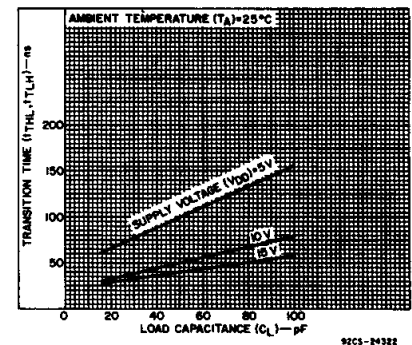


Fig. 6—Typical transition time as a function of load capacitance.

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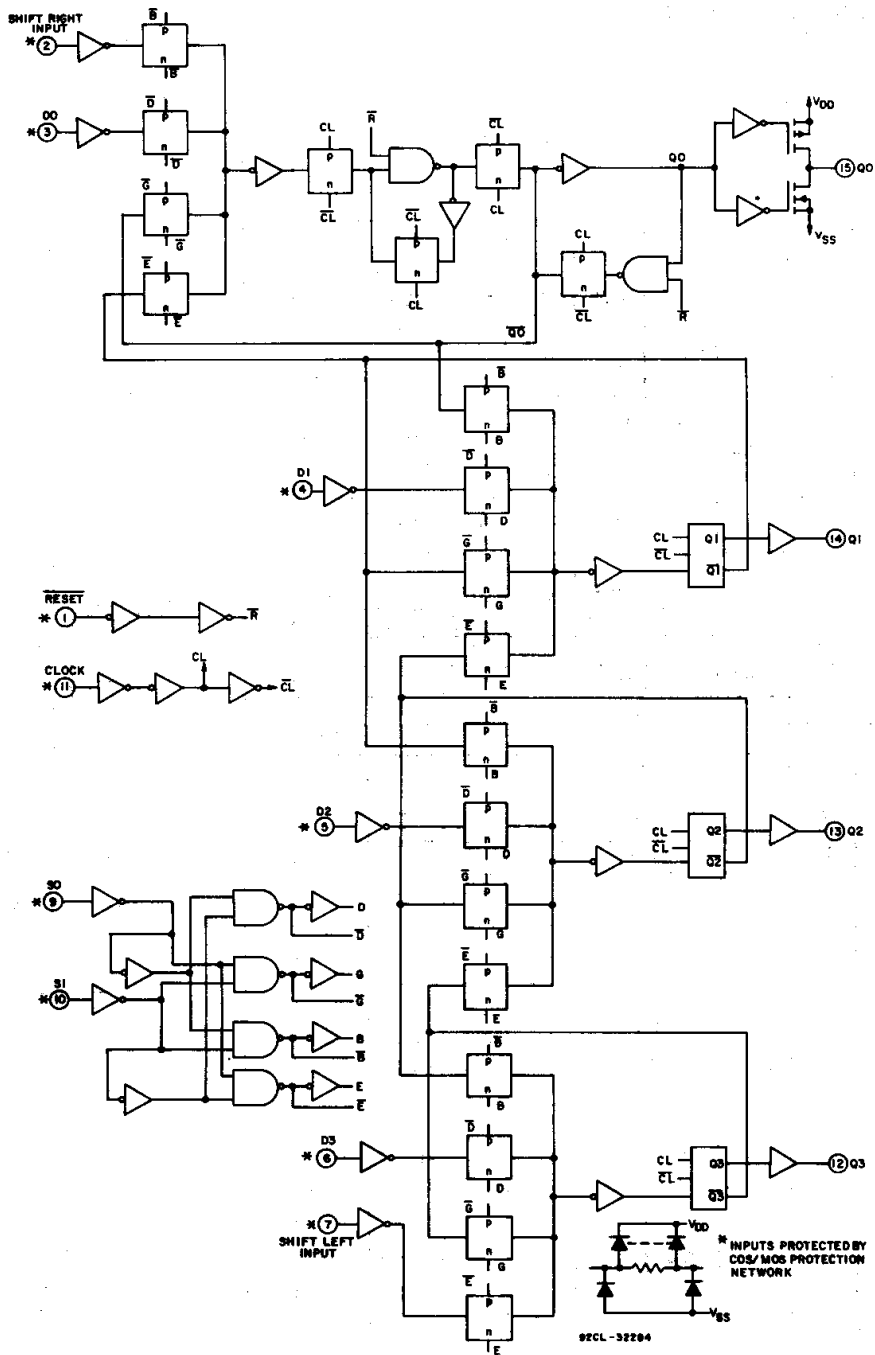


Fig. 8—CD40194B logic diagram.

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	—	0,5	5	5	5	150	150	—	0.04	5	μA
	—	0,10	10	10	10	300	300	—	0.04	10	
	—	0,15	15	20	20	600	600	—	0.04	20	
Output Low (Sink) Current, I _{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.8	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I _{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage: Low-Level, V _{OL} Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V _{OH} Min.	—	0,5	5	4.95				4.95	5	—	V
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage, V _{IL} Max.	0.5, 4.5	—	5	1.5				—	—	1.5	V
	1,9	—	10	3				—	—	3	
	1.5, 13.5	—	15	4				—	—	4	
Input High Voltage, V _{IH} Min.	0.5, 4.5	—	5	3.5				3.5	—	—	V
	1,9	—	10	7				7	—	—	
	1.5, 13.5	—	15	11				11	—	—	
Input Current I _{IN} Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA
3-State Output Leakage Current, I _{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	—	±10 ⁻⁴	±0.4	μA

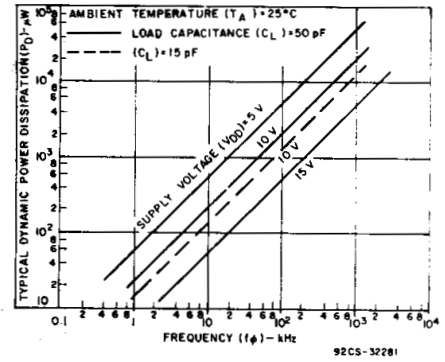


Fig. 9—Typical power dissipation as a function of frequency.

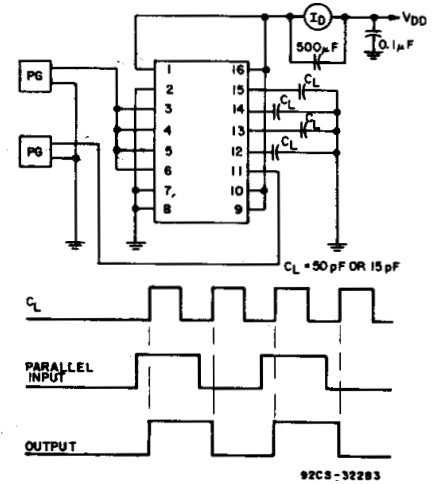


Fig. 10—Dynamic power dissipation test circuit.

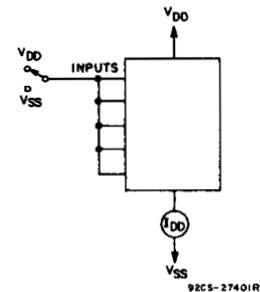


Fig. 11—Quiescent device current test circuit.

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DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$,
 Input $t_r, t_f = 20 \text{ ns}$, $C_L = 50 \text{ pF}$, $R_L = 200 \text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS	
		VDD V	Min.	Typ.		Max.
Propagation Delay Time: Clock to Q t_{PHL}, t_{PLH}		5	—	220	440	ns
		10	—	100	200	
		15	—	70	140	
Output Transition Time t_{THL}, t_{TLH}		5	—	100	200	
		10	—	50	100	
		15	—	40	80	
Minimum Setup Time: t_s D0, D3, SR _{IN} , SL _{IN} to Clock		5	—	80	160	
		10	—	35	70	
		15	—	20	50	
SELECT 0, SELECT 1 to Clock		5	—	200	400	
		10	—	110	220	
		15	—	65	130	
Minimum Hold Time: t_H D0, D3, SR _{IN} , SL _{IN} to Clock		5	—	-65	0	
		10	—	-25	0	
		15	—	-15	0	
SELECT 0, SELECT 1 to Clock		5	—	-170	0	
		10	—	-95	0	
		15	—	-55	0	
Minimum Clock Pulse Width t_w		5	—	90	180	
		10	—	40	80	
		15	—	25	50	
Maximum Clock Input Frequency f_{CL}		5	3	6	—	MHz
		10	6	12	—	
		15	8	15	—	
Maximum Clock Rise or Fall Time t_{rCL}, t_{fCL}		5	—	—	1000	μs
		10	—	—	100	
		15	—	—	100	
Minimum Reset Pulse Width* t_{WR}		5	—	150	300	ns
		10	—	100	200	
		15	—	70	140	
Reset Propagation Delay t_{PRHL}		5	—	230	460	
		10	—	90	180	
		15	—	65	130	
Input Capacitance C_{IN}	Any Input		—	5	7.5	pF

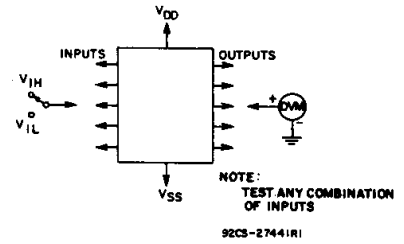


Fig. 12—Input-voltage test circuit.

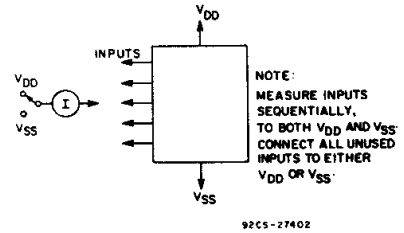
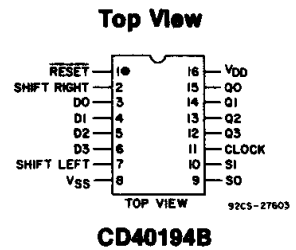


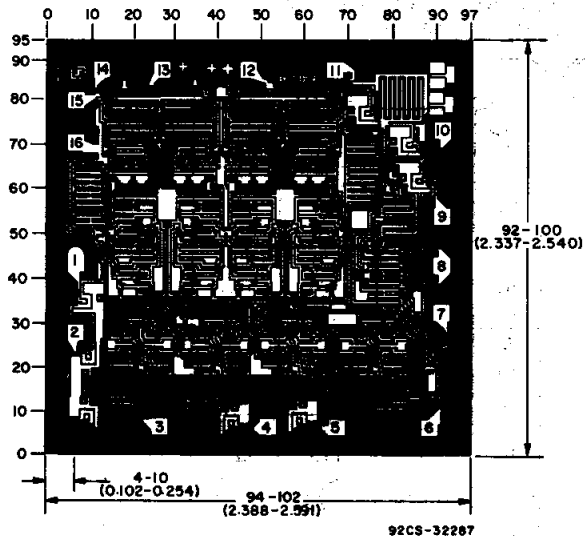
Fig. 13—Input current test circuit.

TERMINAL DIAGRAM



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Dimensions and pad layout for CD40194BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD40194BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD40194BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40194BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40194BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40194BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40194BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40194BPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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