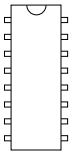
A6800/A6801

Datasheet
26180.110c

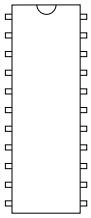
DABiC-5 Latched Sink Drivers

A6800SA

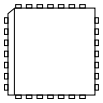


A6800SL

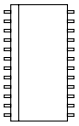
A6801SA



A6801SEP



A6801SLW



ABSOLUTE MAXIMUM RATINGS

Output Voltage, V_{CE} ..... **50 V**
Supply Voltage, V_{DD} ..... **7 V**
Input Voltage Range, V_{IN} ..... **–0.3 V to V_{DD} +0.3 V**
Continuous Collector Current, I_C ..... **600 mA**
Package Power Dissipation, P_D, *see* Allowable Power Disspation chart, page 5
Operating Temperature Range
Ambient Temperature, T_A ..... **–20°C to +85°C**
Storage Temperature, T_S ..... **–55°C to +150°C**

Caution: CMOS devices have input-static protection, but are susceptible to damage when exposed to extremely high static-electrical charges.

The A6800 and A6801 latched-input BiMOS ICs merge high-current, high-voltage outputs with CMOS logic. The CMOS input section consists of 4 or 8 data ('D' type) latches with associated common CLEAR, STROBE, and OUTPUT ENABLE circuitry. The power outputs are bipolar NPN Darlingtons. This merged technology provides versatile, flexible interface. These BiMOS power interface ICs greatly benefit the simplification of computer or microprocessor I/O. The A6800 ICs each contain four latched drivers. A6801 ICs contain eight latched drivers.

The CMOS inputs are compatible with standard CMOS circuits. TTL circuits may mandate the addition of input pull-up resistors. The bipolar Darlington outputs are suitable for directly driving many peripheral/ power loads: relays, lamps, solenoids, small dc motors, etc.

All devices have open-collector outputs and integral diodes for inductive load transient suppression. The output transistors are capable of sinking 600 mA and will withstand at least 50 V in the OFF state. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current can only be accomplished by a reduction in duty cycle. Outputs may be paralleled for higher load current capability.

The A6800SA is furnished in a standard 14-pin DIP; the A6800SL and A6801SLW in surface-mountable SOICs; the A6801SA in a 22-pin DIP with 0.400" (10.16 mm) row centers; the A6801SEP in a 28-lead PLCC. These devices are lead (Pb) free, with 100% matte tin plated leadframes.

FEATURES

- 3.3 V to 5 V logic supply range
- To 10 MHz data input rate
- High-voltage, high-current outputs
- Darlington current-sink outputs, with improved low-saturation voltages
- CMOS, TTL compatible inputs
- Output transient protection
- Internal pull-down resistors
- Low-power CMOS latches

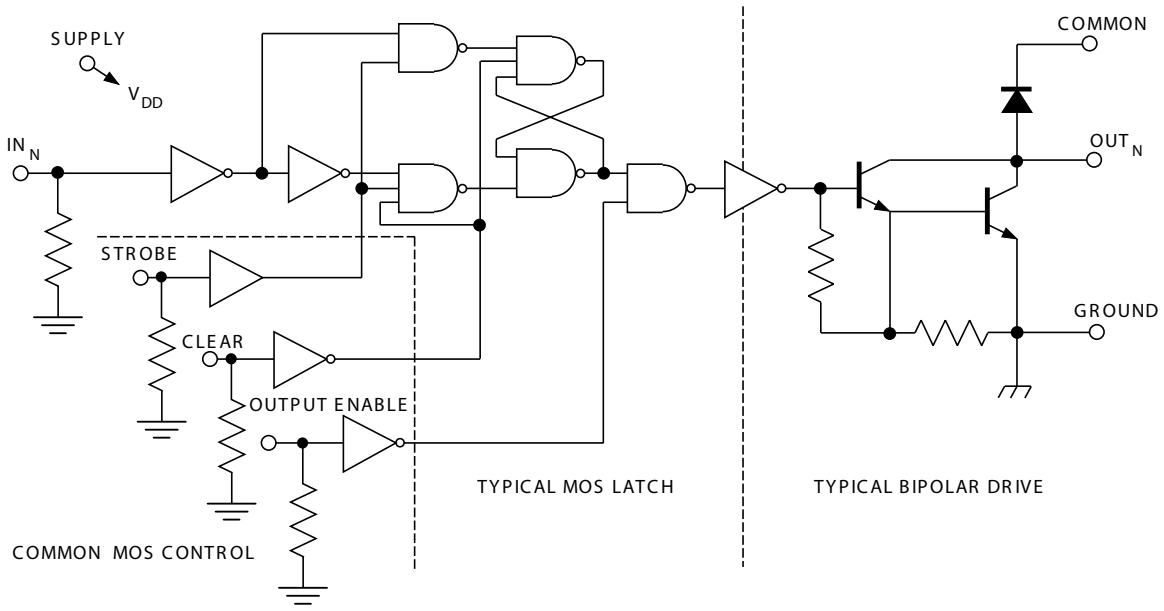
APPLICATIONS

- Relays
- Lamps
- Solenoids
- Small dc motors

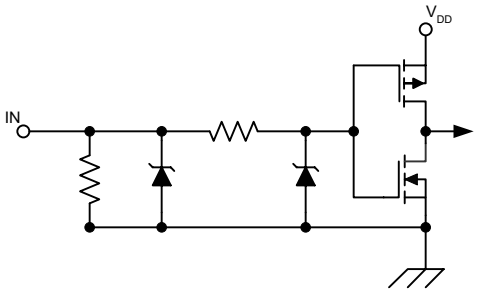
Use the following complete part numbers when ordering:

Part Number	Pins	Package
A6800SA-T	14	DIP
A6800SL-T	14	SOIC
A6801SA-T	22	DIP
A6801SEP-T	28	PLCC
A6801SLW-T	24	SOIC

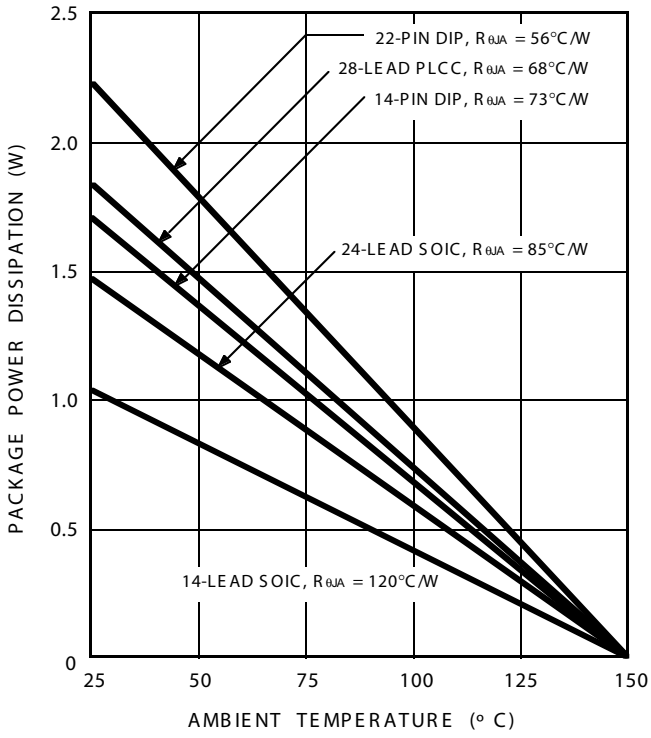
Functional Block Diagram



Typical Input Circuit



Allowable Power Dissipation



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ELECTRICAL CHARACTERISTICS[1] Unless otherwise noted: T_A = 25°C, logic supply operating voltage V_{dd} = 3.0 V to 5.5 V

Characteristic	Symbol	Test Conditions	V_{dd} = 3.3 V			V_{dd} = 5 V			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{OUT} = 50 V	–	–	10	–	–	10	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	I_{OUT} = 350 mA, L = 3 mH	35	–	–	35	–	–	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 100 mA	–	0.8	1.0	–	0.8	1.0	V
		I_{OUT} = 200 mA	–	0.9	1.1	–	0.9	1.1	V
		I_{OUT} = 350 mA (See note 2)	–	1.0	1.3	–	1.0	1.3	V
Input Voltage	$V_{IN(1)}$		2.2	–	–	3.3	–	–	V
	$V_{IN(0)}$		–	–	1.1	–	–	1.7	V
Input Resistance	R_{IN}		50	–	–	50	–	–	kΩ
Logic Supply Current	$I_{DD(1)}$	One output on, I_{OUT} = 100 mA	–	–	1.0	–	–	1.0	mA
	$I_{DD(0)}$	All outputs off	–	130	150	–	130	150	µA
Clamp Diode Leakage Current	I_r	V_r = 50 V	–	–	50	–	–	50	µA
Clamp Diode Forward Voltage	V_f	I_f = 350 mA	–	–	2.0	–	–	2.0	V
Output Fall Time	t_f	V_{CC} = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	80	–	–	80	–	ns
Output Rise Time	t_r	V_{CC} = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	100	–	–	100	–	ns

[1] Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure a minimum logic 1.
[2] Because of limitations on package power dissipation, the simultaneous operation of multiple drivers can only be accomplished by reduction in duty cycle.

Truth Table

IN_N	STROBE	CLEAR	OUTPUT ENABLE	OUT_N	
				t-1	t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

X = irrelevant
t-1 = previous output state
t = present output state

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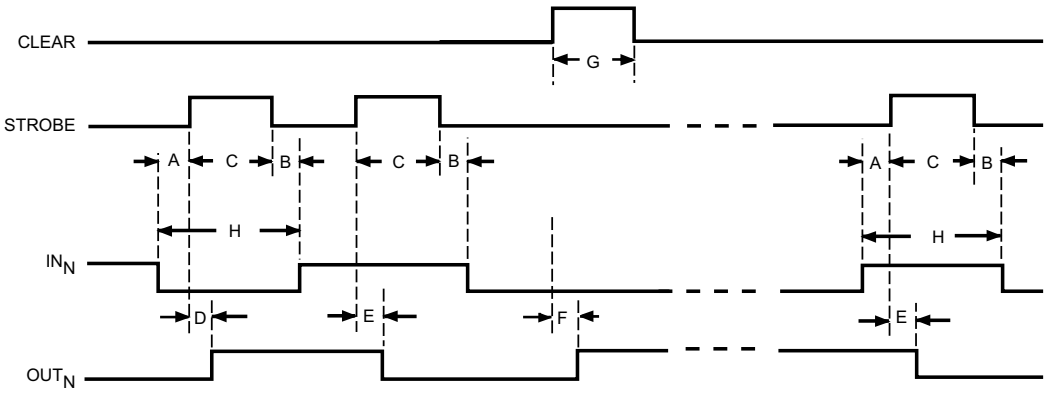
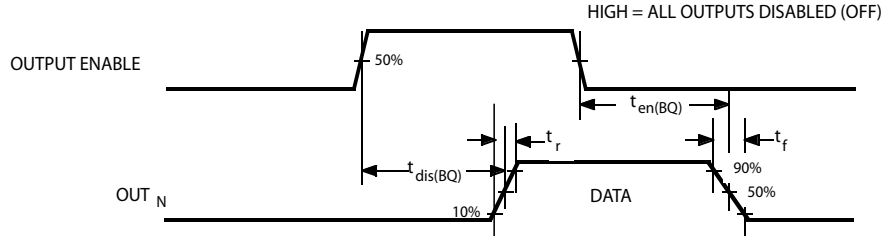
Timing Requirements and Specifications
(Logic Levels are V_{DD} and Ground)





Key	Description	Time (ns)
A	Minimum data active time before Strobe enabled (Data Set-Up Time)	25
B	Minimum data active time after Strobe disabled (Data Hold Time)	25
C	Minimum Strobe pulse width	50
D	Maximum time between Strobe activation and transition from output on to output off*	500
E	Maximum time between Strobe activation and transition from output off to output on*	500
F	Maximum time between Clear activation and transition from output on to output off*	500
G	Minimum Clear pulse width	50
H	Minimum data pulse width	100
$t_{dis(BQ)}$	Output Enable to output off delay*	500
$t_{en(BQ)}$	Output Enable to output on delay*	500

*Conditions for output transition testing are: V_{CC} = 50 V, V_{DD} = 5 V, R1 = 500 Ω, C1 ≤ 30 pF.

NOTE: Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output off condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the off condition, regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

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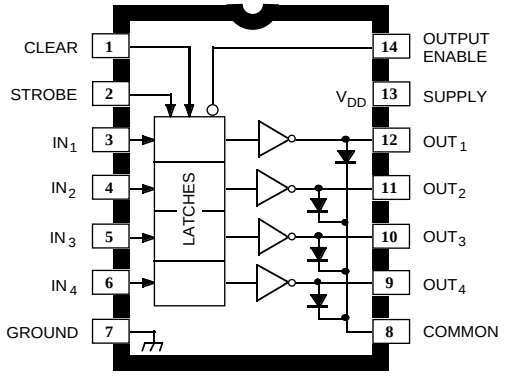
A6800SL

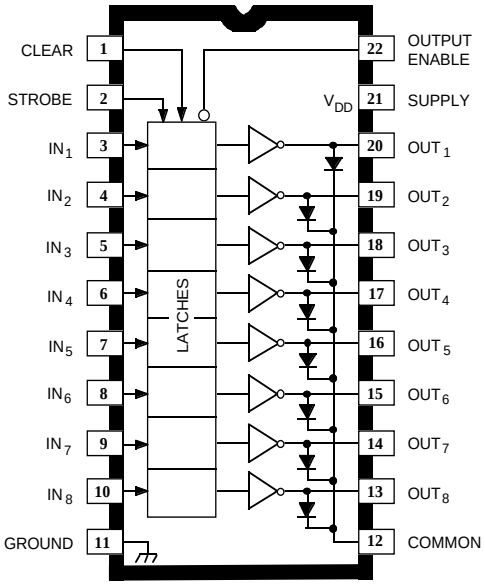
A6800SA



Dwg. PP-014A

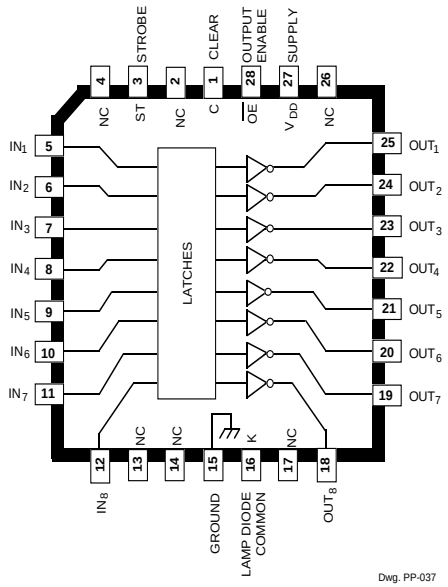
Note: The A6800SL (SOIC) and the A6800SA (DIP) are electrically identical and share a common terminal number assignment.

A6801SA



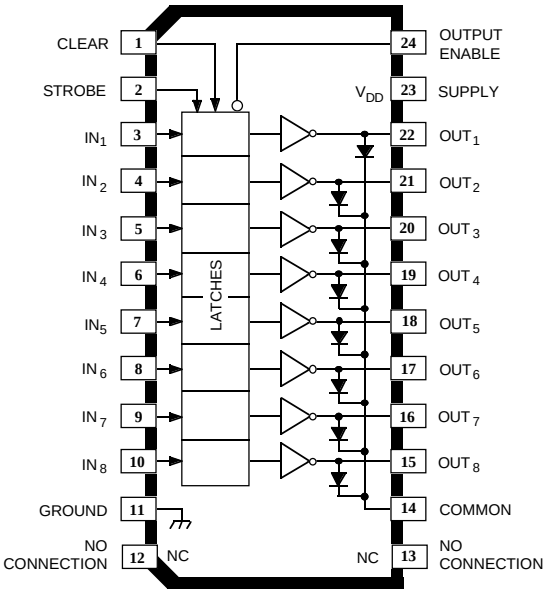
Dwg. PP-015

A6801SEP



Dwg. PP-037

A6801SLW



Dwg. PP-015-1

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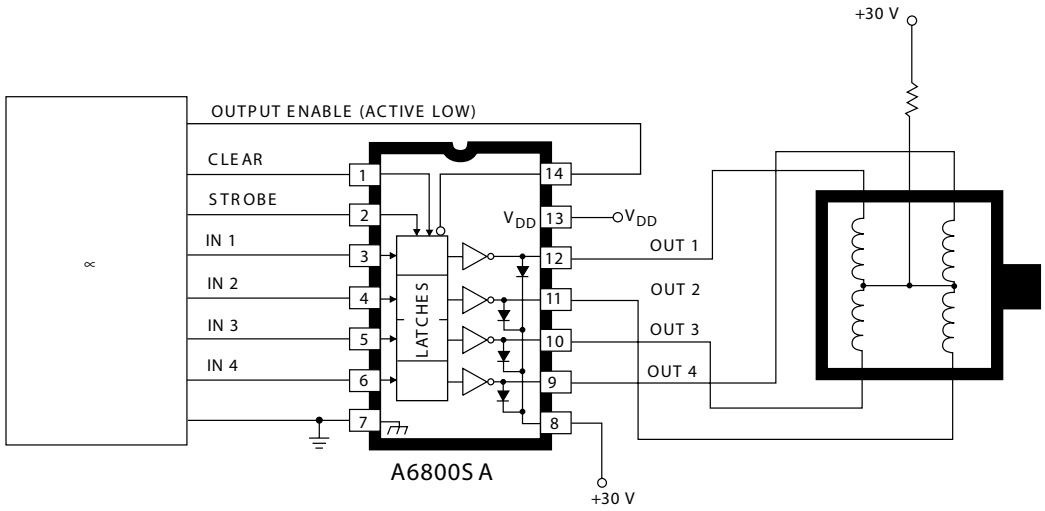
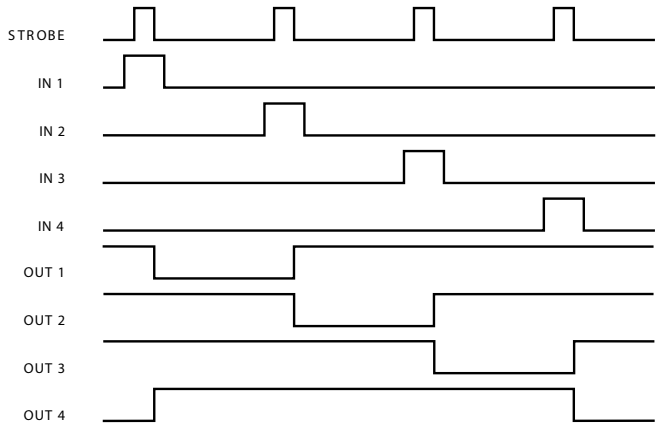
TYPICAL APPLICATION
UNIPOLAR STEPPER-MOTOR DRIVE



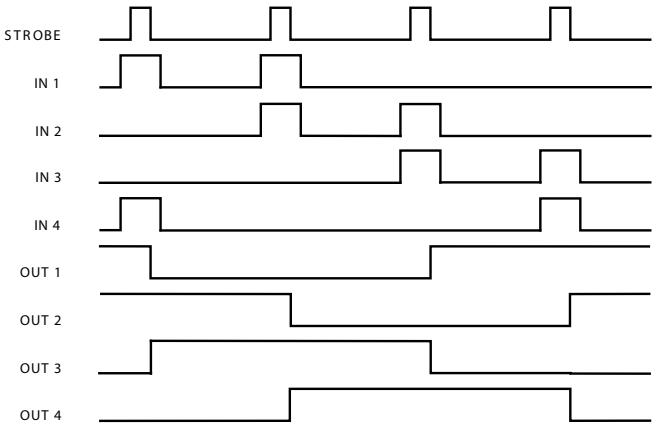
Dwg. No. B-1537

UNIPOLAR WAVE DRIVE



Dwg. GP-060

UNIPOLAR 2-PHASE DRIVE



Dwg. GP-060-1

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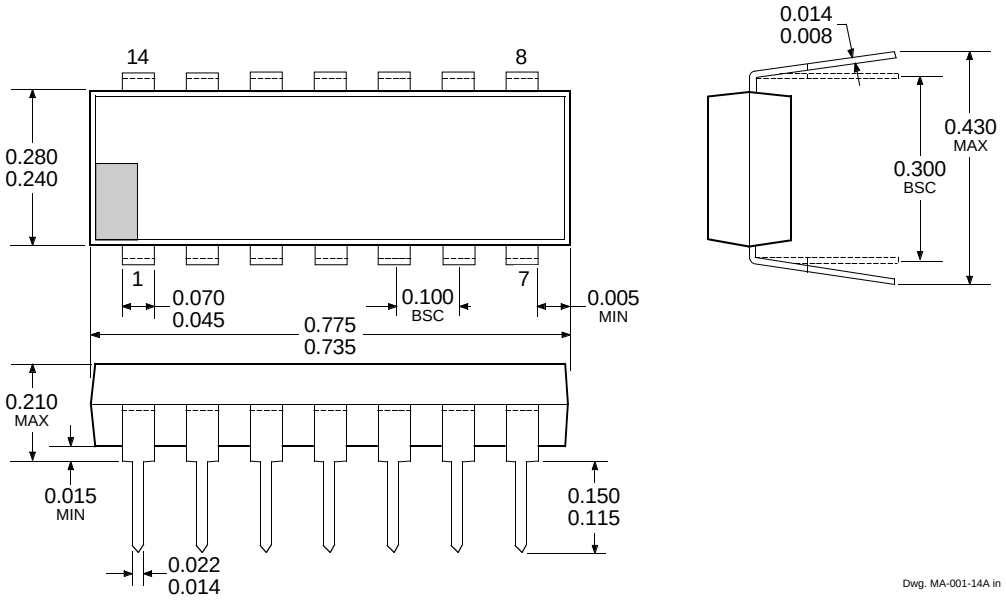
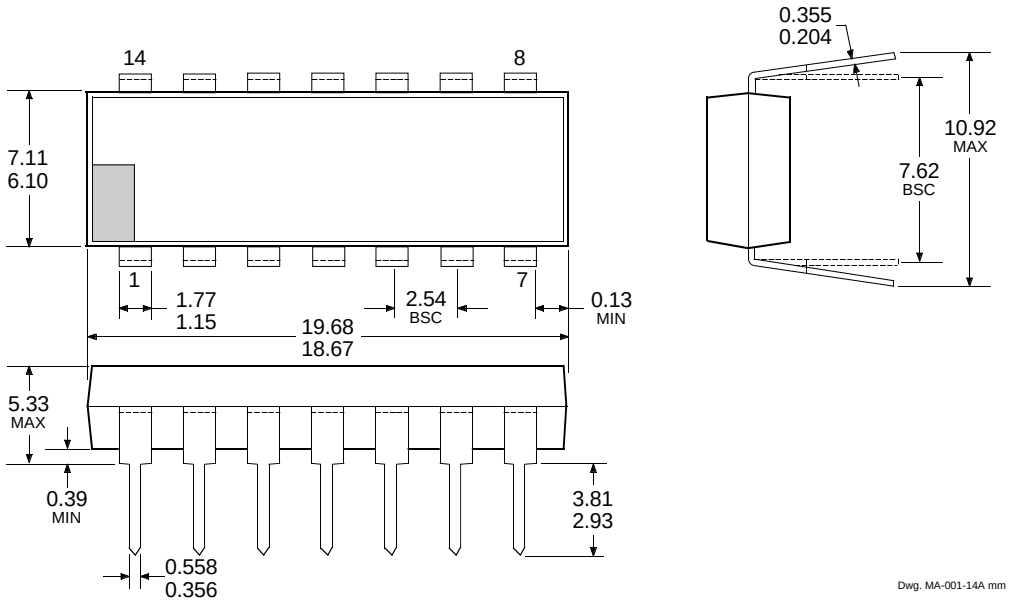
A6800SA

Dimensions in Inches
(controlling dimensions)



Dwg. MA-001-14A in

Dimensions in Millimeters
(for reference only)



Dwg. MA-001-14A mm

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.
3. Lead thickness is measured at seating plane or below.

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A6800SL

Dimensions in Inches
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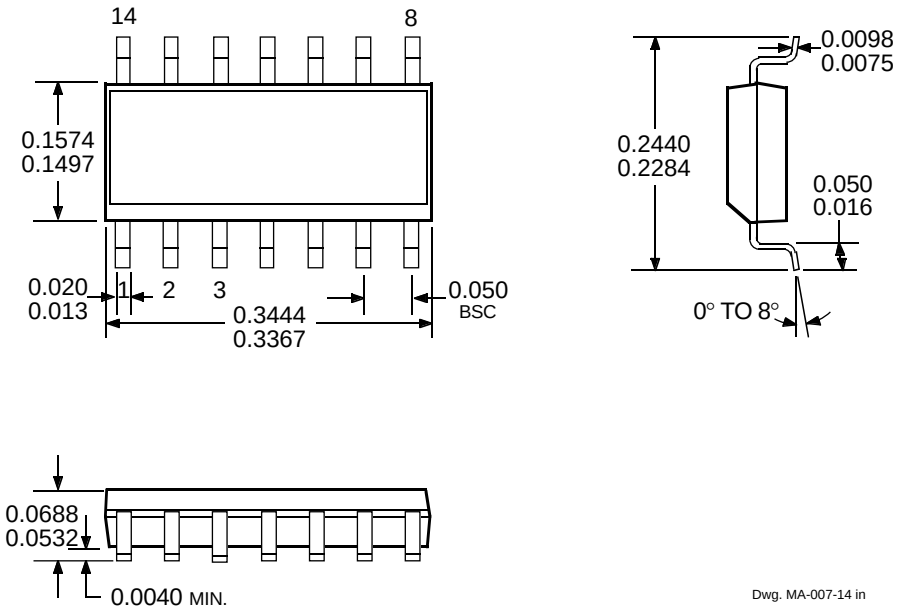

Dwg. MA-007-14 in

Dimensions in Millimeters
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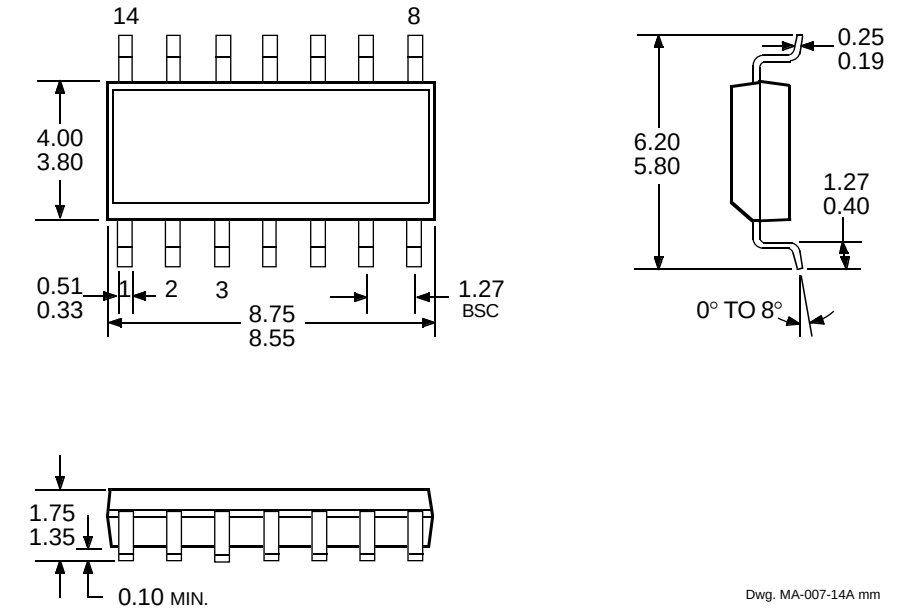

Dwg. MA-007-14A mm

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
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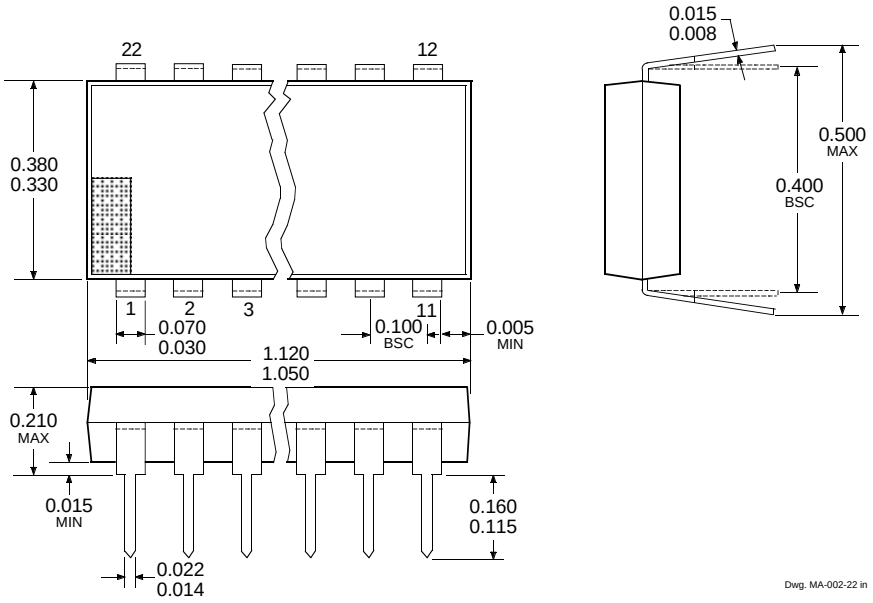
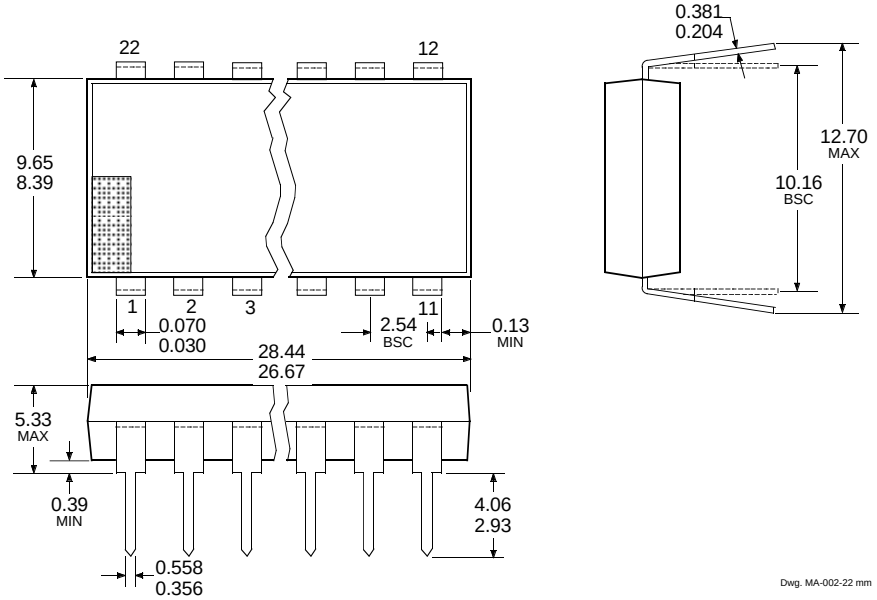
A6801SA

Dimensions in Inches
(controlling dimensions)



Dwg. MA-002-22 in

Dimensions in Millimeters
(for reference only)



Dwg. MA-002-22 mm

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
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A6801SEP

Dimensions in Inches
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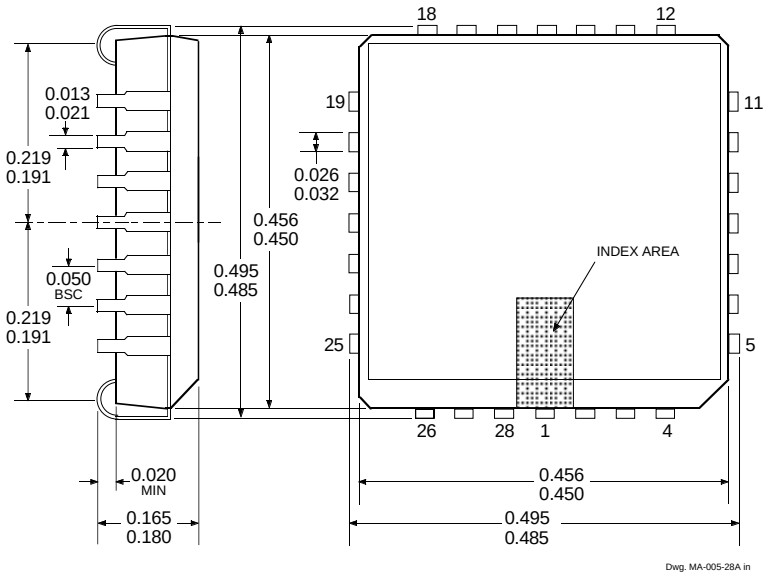
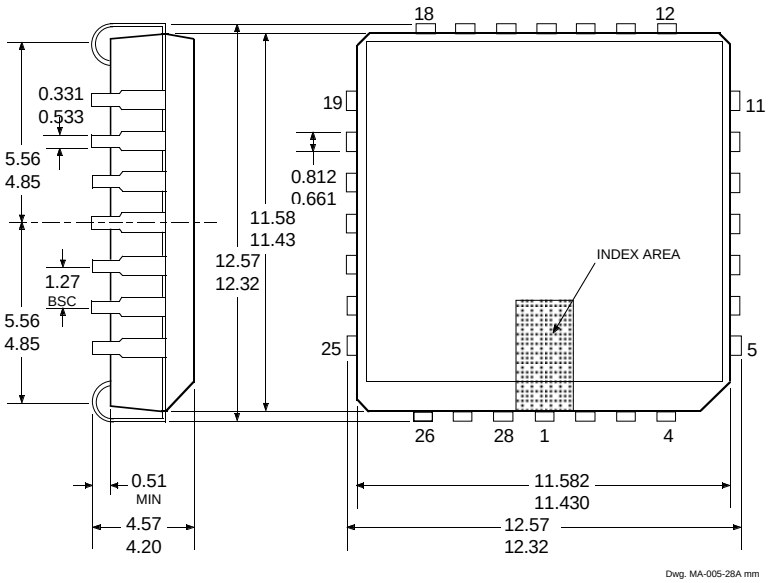


Dimensions in Millimeters
(for reference only)



NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
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A6801SLW

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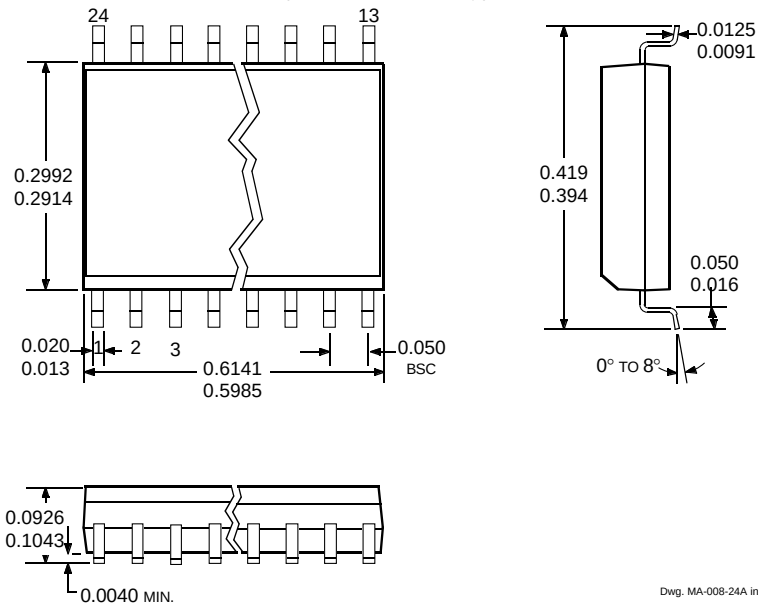
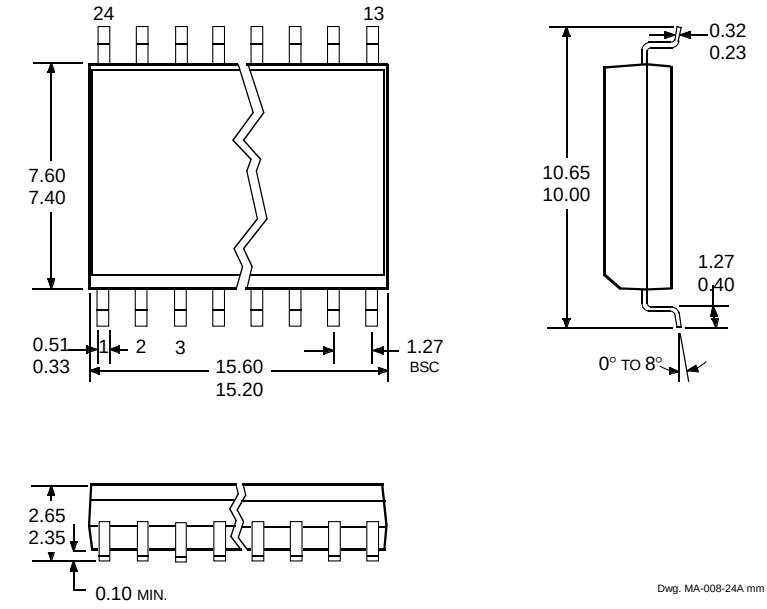


Dwg. MA-008-24A in

Dimensions in Millimeters
(controlling dimensions)



Dwg. MA-008-24A mm

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
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