

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4894B

12-stage shift-and-store register
LED driver

Product specification
File under Integrated Circuits, IC04

January 1995

12-stage shift-and-store register LED driver

HEF4894B

APPLICATIONS

- Automotive
- Industrial

GENERAL DESCRIPTION

The HEF4894B is a 12 stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel LED driver outputs O_0 to O_{11} . Data is shifted on positive-going clock transitions. The data in each shift register stage is transferred to the storage register when the strobe (STR) input is HIGH. Data in the storage register appears at the outputs whenever the output enable (EO) signal is HIGH.

Two serial outputs (O_S and O_S') are available for cascading a number of HEF4894B devices. Data is available at O_S on positive-going clock edges to allow high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information is available at O_S' on the next negative-going clock edge and provides cascading HEF4894B devices when the clock rise time is slow.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PIN POSITION	MATERIAL	CODE
HEF4894BT	20	SO	plastic	SO20/SOT163A
HEF4894BP	20	DIL	plastic	DIL20/SOT146

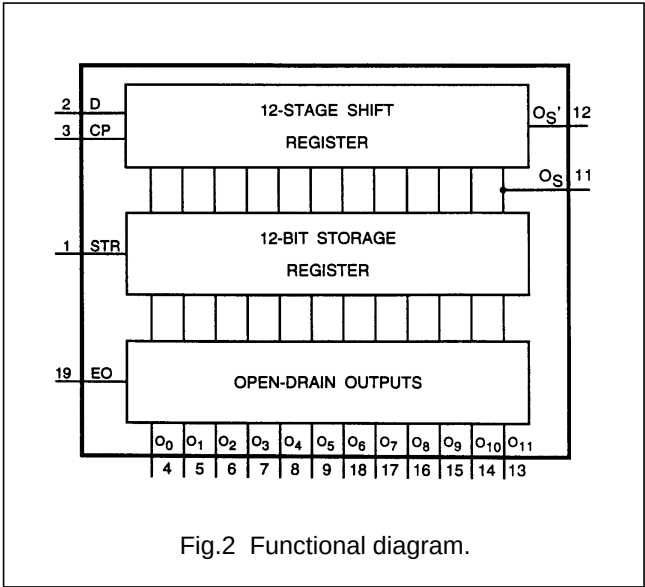
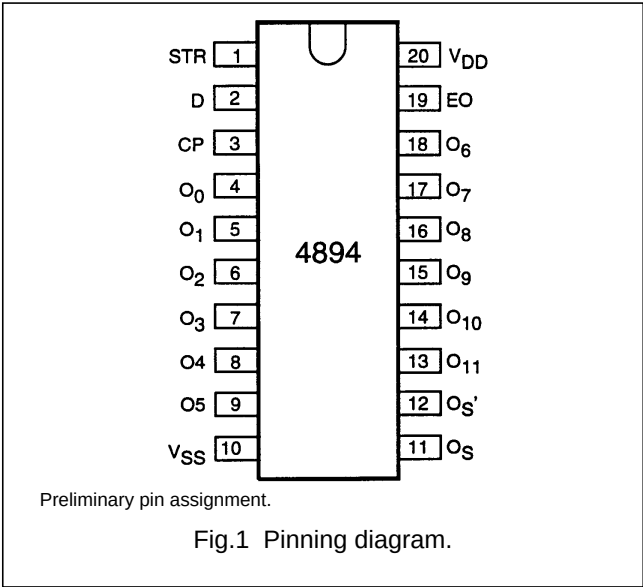
PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	STR	strobe input
2	D	data input
3	CP	clock input
4, 5, 6, 7, 8, 9, 18, 17, 16, 15, 14, 13	O_0 to O_{11}	parallel outputs (open drain)
10	V_{SS}	ground
11, 12	O_S , O_S'	serial outputs
19	EO	output enable input
20	V_{DD}	positive supply voltage

FAMILY DATA

See Family Specifications except for:
Rating for DC current into any open-drain output: 40 mA.

I_{DD} LIMITS category MSI: see Family Specifications.



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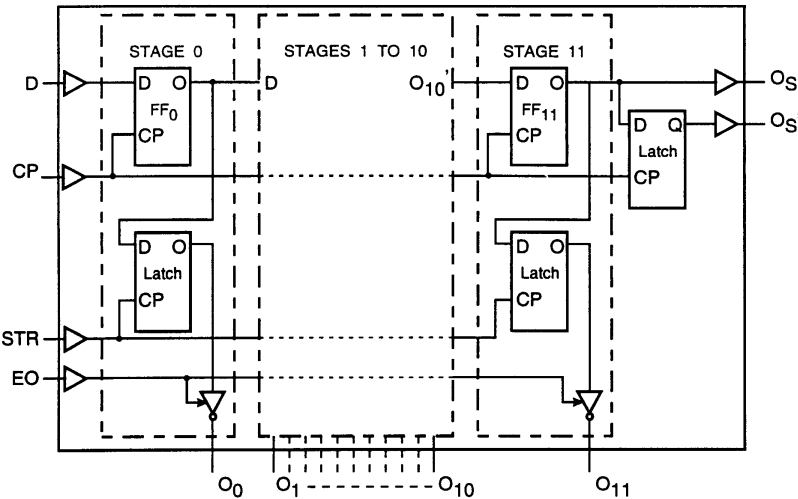


Fig.3 Logic diagram.

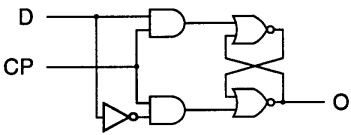


Fig.4 One D-latch.

FUNCTION TABLE

INPUTS				PARALLEL OUTPUTS		SERIAL OUTPUTS	
CP	EO	STR	D	O ₀	O _n	O _S	O _S '
↑	L	X	X	Z	Z	O ₁₀ '	nc
↓	L	X	X	Z	Z	nc	O ₁₁
↑	H	L	X	nc	nc	O ₁₀ '	nc
↑	H	H	L	Z	O _n - 1	O ₁₀ '	nc
↑	H	H	H	L	O _n - 1	O ₁₀ '	nc
↓	H	H	H	nc	nc	nc	O ₁₁

Notes

1. H = HIGH state (the more positive voltage)
2. L = LOW state (the less positive voltage)
3. X = state is immaterial
4. ↑ = positive-going transition
5. ↓ = negative-going transition
6. Z = high impedance OFF state
7. nc = no change
8. O₁₁' = the information in the twelfth shift register stage.

At the positive clock edge the information in the 10th register stage is transferred to the 11th register stage and the O_S output.

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DC CHARACTERISTICS

 $V_{SS} = 0$ V.

PARAMETER	V _{DD} (V)	SYMBOL	T _{amb} (°C)						UNIT	CONDITIONS
			−40		+ 25		+ 85			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
output voltage LOW; O _n	5	V _{OL}	−	0.75	−	0.75	−	1.5	V	V _I = V _{SS} or V _{DD} ; I _o < 20 mA
	10		−	0.75	−	0.75	−	1.5		
	15		−	0.75	−	0.75	−	1.5		
output leakage current; HIGH; O _n	5	I _{OZH}	−	2	−	2	−	15	μA	V _o = 15 V
	10		−	2	−	2	−	15		
	15		−	2	−	2	−	15		

AC CHARACTERISTICS

 $V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ≤ 20 ns.

PARAMETER	V_{DD} (V)	TYPICAL FORMULA FOR P (μ W)	
Dynamic power dissipation per package (P)	5	$1200 f_i + \sum(f_o C_L) \times V_{DD}^2$	where: $R_{load} = \infty$ f_i = input frequency (MHz), f_o = output frequency (MHz), C_L = load capacitance (pF), $\sum(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$5550 f_i + \sum(f_o C_L) \times V_{DD}^2$	
	15	$15000 f_i + \sum(f_o C_L) \times V_{DD}^2$	

AC CHARACTERISTICS

 $V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns.

PARAMETER	V_{DD} (V)	SYMBOL	TYP.	MAX.	UNIT	TYPICAL EXTRAPOLATION FORMULA
Propagation delay CP to O_s HIGH to LOW	5 10 15	t_{PHL}	160 65 45	320 130 90	ns	132 ns + (0.55 ns/pF) C_L 53 ns + (0.23 ns/pF) C_L 37 ns + (0.16 ns/pF) C_L
Propagation delay CP to O_s LOW to HIGH	5 10 15	t_{PLH}	130 55 40	260 110 80	ns	102 ns + (0.55 ns/pF) C_L 44 ns + (0.23 ns/pF) C_L 32 ns + (0.16 ns/pF) C_L
Propagation delay CP to O_s' HIGH to LOW	5 10 15	t_{PHL}	120 50 40	240 100 80	ns	92 ns + (0.55 ns/pF) C_L 39 ns + (0.23 ns/pF) C_L 32 ns + (0.16 ns/pF) C_L
Propagation delay CP to O_s' LOW to HIGH	5 10 15	t_{PLH}	130 60 45	260 120 90	ns	102 ns + (0.55 ns/pF) C_L 49 ns + (0.23 ns/pF) C_L 37 ns + (0.16 ns/pF) C_L

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PARAMETER	V _{DD} (V)	SYMBOL	TYP.	MAX.	UNIT	TYPICAL EXTRAPOLATION FORMULA
Propagation delay CP to O _n OFF to LOW	5 10 15	t _{PZL}	240 80 55	480 160 110	ns	see note 1
Propagation delay CP to O _n LOW to OFF	5 10 15	t _{PLZ}	170 75 60	340 150 120	ns	see note 1
Propagation delay STR to O _n OFF to LOW	5 10 15	t _{PZL}	140 70 55	280 140 110	ns	see note 1
Propagation delay STR to O _n LOW to OFF	5 10 15	t _{PLZ}	100 40 35	200 100 70	ns	see note 1
Output transition time; O _s , O _s ' HIGH to LOW	5 10 15	t _{THL}	85 40 30	170 80 60	ns	35 ns + (1.0 ns/pF) C _L 19 ns + (0.42 ns/pF) C _L 16 ns + (0.28 ns/pF) C _L
Output transition time; O _s , O _s ' LOW to HIGH	5 10 15	t _{TLH}	85 40 30	170 80 60	ns	35 ns + (1.0 ns/pF) C _L 19 ns + (0.42 ns/pF) C _L 16 ns + (0.28 ns/pF) C _L

Note

1. Definition of symbol equivalent to 3-state outputs.

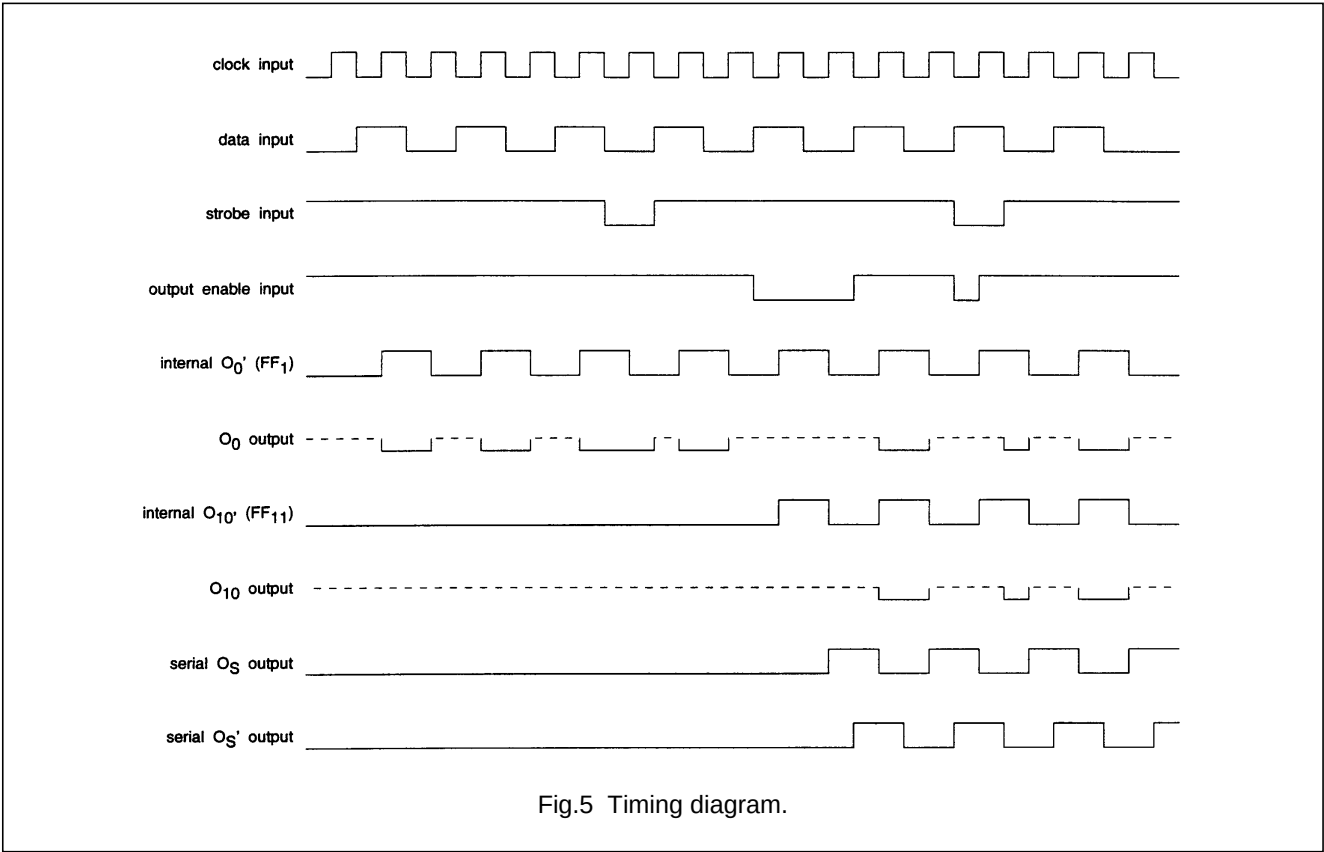
AC CHARACTERISTICSV_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns.

PARAMETER	V _{DD} (V)	SYMBOL	MIN.	TYP.	MAX.	UNIT
output enable time EO to O _n OFF to LOW	5 10 15	t _{PZL}	— — —	100 55 50	200 110 100	ns
output disable time EO to O _n LOW to OFF	5 10 15	t _{PLZ}	— — —	80 40 30	160 80 60	ns
minimum clock pulse width LOW	5 10 15	t _{WCPL}	60 30 24	30 15 12	— — —	ns
minimum strobe pulse width HIGH	5 10 15	t _{WSTRH}	80 60 24	40 30 12	— — —	ns

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PARAMETER	V _{DD} (V)	SYMBOL	MIN.	TYP.	MAX.	UNIT
set-up time D to CP	5	t _{su}	60	30	–	ns
	10		20	10	–	
	15		15	5	–	
hold time D to CP	5	t _{hold}	5	–15	–	ns
	10		20	5	–	
	15		20	5	–	
Maximum clock pulse frequency	5	f _{max}	5	10	–	MHz
	10		11	22	–	
	15		14	28	–	



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APPLICATION INFORMATION

An example of applications for the HEF4894B is:

- Serial-to-parallel converting LED driver

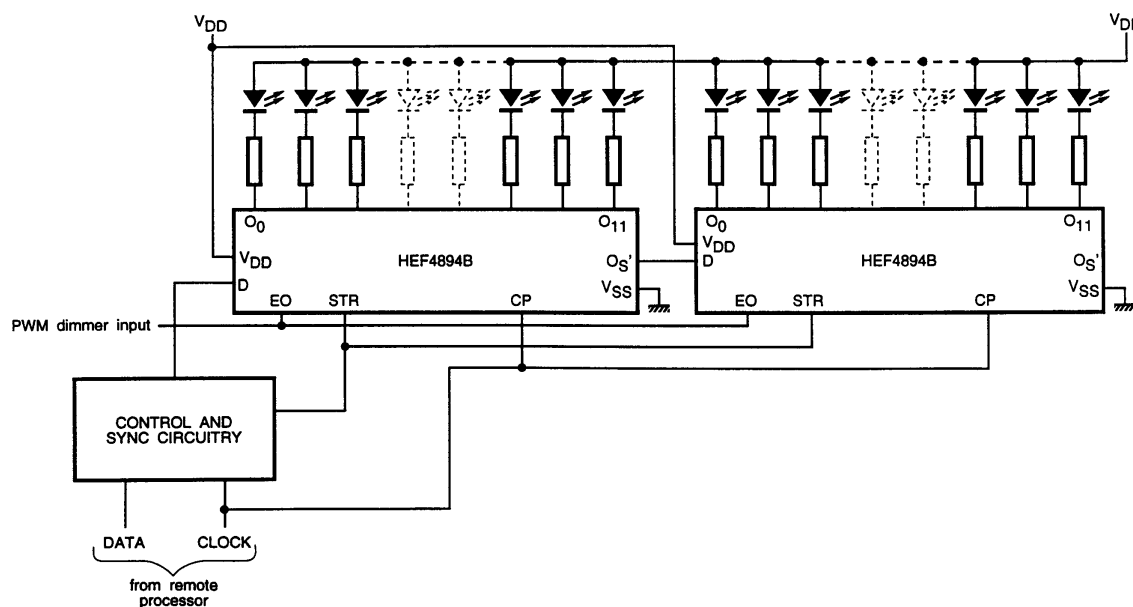


Fig.6 LED driver register.

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