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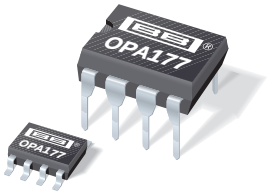



# OPA177

# Precision OPERATIONAL AMPLIFIER

## FEATURES

- LOW OFFSET VOLTAGE: 25μV max
- LOW DRIFT: 0.3μV/°C
- HIGH OPEN-LOOP GAIN: 130dB min
- LOW QUIESCENT CURRENT: 1.5mA typ
- REPLACES INDUSTRY-STANDARD OP AMPS: OP-07, OP-77, OP-177, AD707, ETC.

## APPLICATIONS

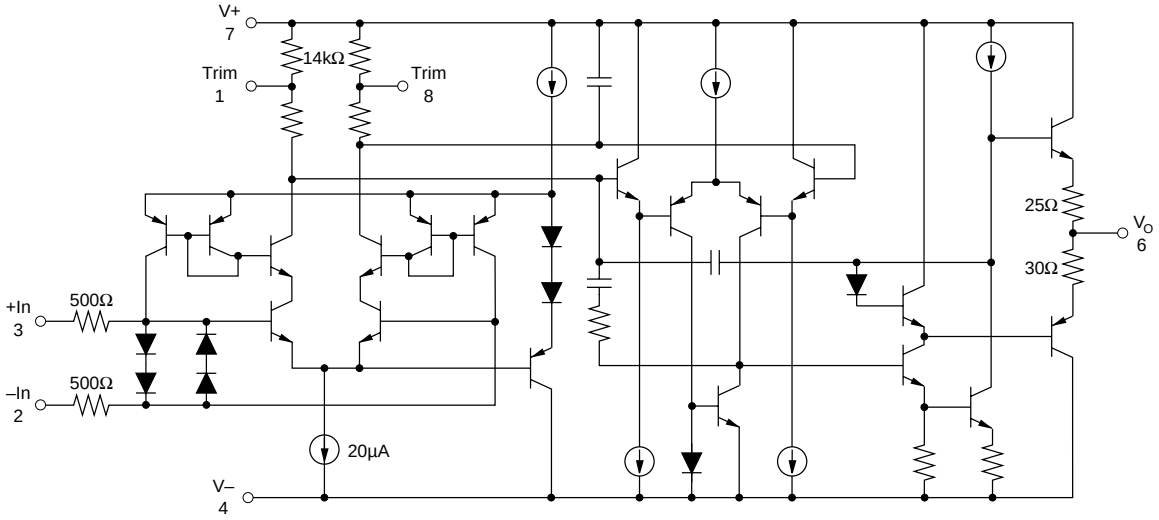
- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER

## DESCRIPTION

The OPA177 precision bipolar op amp feature very low offset voltage and drift. Laser-trimmed offset, drift and input bias current virtually eliminate the need for costly external trimming. The high performance and low cost make them ideally suited to a wide range of precision instrumentation.

The low quiescent current of the OPA177 dramatically reduce warm-up drift and errors due to thermoelectric effects in input interconnections. It provides an effective alternative to chopper-stabilized amplifiers. The low noise of the OPA177 maintains accuracy.

OPA177 performance gradeouts are available. Packaging options include 8-pin plastic DIP and SO-8 surface-mount packages.

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SBOS008

# OPA177 SPECIFICATIONS

At $V_S$ = ±15V, $T_A$ = +25°C, unless otherwise noted.

| PARAMETER | CONDITION | OPA177F MIN | OPA177F TYP | OPA177F MAX | OPA177G MIN | OPA177G TYP | OPA177G MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | | |
| Input Offset Voltage | | | 10 | 25 | | 20 | 60 | µV |
| Long-Term Input Offset[1] Voltage Stability | | | 0.3 | | | 0.4 | | µV/Mo |
| Offset Adjustment Range | $R_P$ = 20kΩ | | ±3 | | | * | | mV |
| Power Supply Rejection Ratio | $V_S$ = ±3V to ±18V | 115 | 125 | | 110 | 120 | | dB |
| **INPUT BIAS CURRENT** | | | | | | | | |
| Input Offset Current | | | 0.3 | 1.5 | | * | 2.8 | nA |
| Input Bias Current | | | 0.5 | ±2 | | * | ±2.8 | nA |
| **NOISE** | | | | | | | | |
| Input Noise Voltage | 1Hz to 100Hz[2] | | 85 | 150 | | * | * | nVrms |
| Input Noise Current | 1Hz to 100Hz | | 4.5 | | | * | | pArms |
| **INPUT IMPEDANCE** | | | | | | | | |
| Input Resistance | Differential Mode[3] | 26 | 45 | | 18.5 | * | | MΩ |
| | Common-Mode | | 200 | | | * | | GΩ |
| **INPUT VOLTAGE RANGE** | | | | | | | | |
| Common-Mode Input Range[4] | | ±13 | ±14 | | * | * | | V |
| Common-Mode Rejection | $V_{CM}$ = ±13V | 130 | 140 | | 115 | * | | dB |
| **OPEN-LOOP GAIN** | $R_L$ ≥ 2kΩ | | | | | | | |
| Large Signal Voltage Gain | $V_O$ = ±10V[5] | 5110 | 12,000 | | 2000 | 6000 | | V/mV |
| **OUTPUT** | | | | | | | | |
| Output Voltage Swing | $R_L$ ≥ 10kΩ | ±13.5 | ±14 | | * | * | | V |
| | $R_L$ ≥ 2kΩ | ±12.5 | ±13 | | * | * | | V |
| | $R_L$ ≥ 1kΩ | ±12 | ±12.5 | | * | * | | V |
| Open-Loop Output Resistance | | | 60 | | | * | | Ω |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Slew Rate | $R_L$ ≥ 2kΩ | 0.1 | 0.3 | | * | * | | V/µs |
| Closed-Loop Bandwidth | G = +1 | 0.4 | 0.6 | | * | * | | MHz |
| **POWER SUPPLY** | | | | | | | | |
| Power Consumption | $V_S$ = ±15V, No Load | | 40 | 60 | | * | * | mW |
| | $V_S$ = ±3V, No Load | | 3.5 | 4.5 | | * | * | mW |
| Supply Current | $V_S$ = ±15V, No Load | | 1.3 | 2 | | * | * | mA |

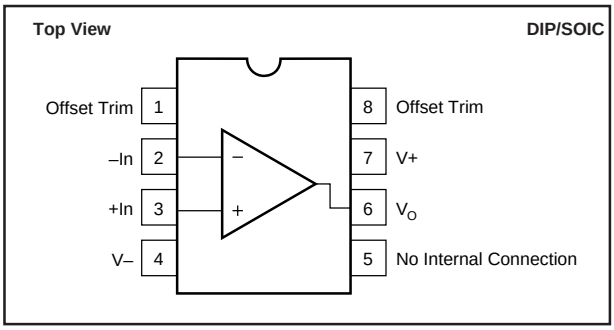
At $V_S$ = ±15V, –40°C ≤ $T_A$ ≤ +85°C, unless otherwise noted.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | | |
| Input Offset Voltage | | | 15 | 40 | | 20 | 100 | µV |
| Average Input Offset Voltage Drift | | | 0.1 | 0.3 | | 0.7 | 1.2 | µV/°C |
| Power Supply Rejection Ratio | $V_S$ = ±3V to ±18V | 110 | 120 | | 106 | 115 | | dB |
| **INPUT BIAS CURRENT** | | | | | | | | |
| Input Offset Current | | | 0.5 | 2.2 | | * | 4.5 | nA |
| Average Input Offset Current Drift[6] | | | 1.5 | 40 | | * | 85 | pA/°C |
| Input Bias Current | | | 0.5 | ±4 | | * | ±6 | nA |
| Average Input Bias Current Drift[6] | | | 8 | 40 | | 15 | 60 | pA/°C |
| **INPUT VOLTAGE RANGE** | | | | | | | | |
| Common-Mode Input Range | | ±13 | ±13.5 | | * | * | | V |
| Common-Mode Rejection | $V_{CM}$ = ±13V | 120 | 140 | | 110 | * | | dB |
| **OPEN-LOOP GAIN** | | | | | | | | |
| Large Signal Voltage Gain | $R_L$ ≥ 2kΩ, $V_O$ = ±10V | 2000 | 6000 | | 1000 | 4000 | | V/mV |
| **OUTPUT** | | | | | | | | |
| Output Voltage Swing | $R_L$ ≥ 2kΩ | ±12 | ±13 | | * | * | | V |
| **POWER SUPPLY** | | | | | | | | |
| Power Consumption | $V_S$ = ±15V, No Load | | 60 | 75 | | * | * | mW |
| Supply Current | $V_S$ = ±15V, No Load | | 2 | 25 | | * | * | mA |

* Same as specification for product to left.

NOTES: (1) Long-Term Input Offset Voltage Stability refers to the averaged trend line of $V_{OS}$ vs time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in $V_{OS}$ during the first 30 operating days are typically less than 2µV. (2) Sample tested. (3) Guaranteed by design. (4) Guaranteed by CMRR test condition. (5) To insure high open-loop gain throughout the ±10V output range, $A_{OL}$ is tested at –10V ≤ $V_O$ ≤ 0V, 0V ≤ $V_O$ ≤ +10V, and –10V ≤ $V_O$ ≤ +10V. (6) Guaranteed by end-point limits.

## PIN CONFIGURATION




## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Voltage | ±22V |
| Differential Input Voltage | ±30V |
| Input Voltage | $\pm V_S$ |
| Output Short Circuit | Continuous |
| Operating Temperature: | |
| Plastic DIP (P), SO-8 (S) | –40°C to +85°C |
| $\theta_{JA}$ (PDIP) | 100°C/W |
| $\theta_{JA}$ (SOIC) | 160°C/W |
| Storage Temperature: | |
| Plastic DIP (P), SO-8 (S) | –65°C to +125°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 10s) P packages | +300°C |
| (soldering, 3s) S package | +260°C |

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| OPA177FP | 8-Pin Plastic DIP | 006 | –40°C to +85°C |
| OPA177GP | 8-Pin Plastic DIP | 006 | –40°C to +85°C |
| OPA177GS | SO-8 Surface-Mount | 182 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. ESD can cause damage ranging from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

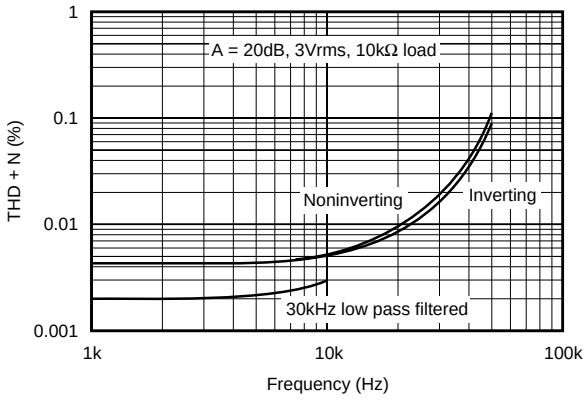
Burr-Brown's standard ESD test method consists of five 1000V positive and negative discharges (100pF in series with 1.5kΩ) applied to each pin.

Failure to observe proper handling procedures could result in small changes to the OPA177's input bias current.

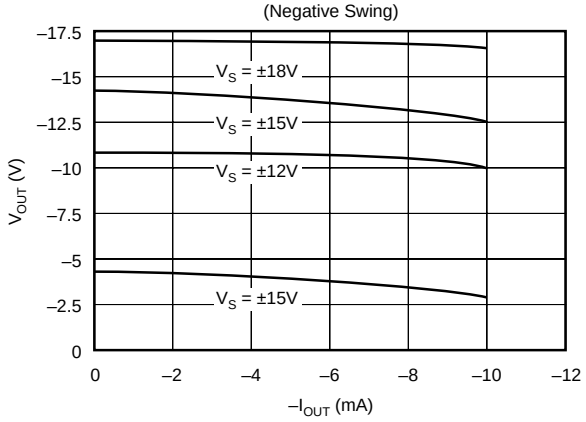
# TYPICAL PERFORMANCE CURVES

At $T_A$ = +25°C, $V_S$ = ±15V, unless otherwise noted.

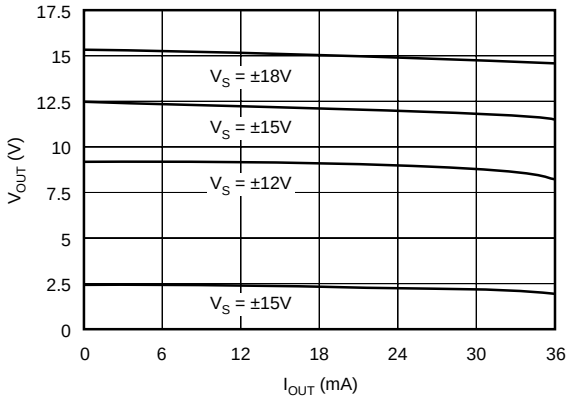
TOTAL HARMONIC DISTORTION AND NOISE vs FREQUENCY



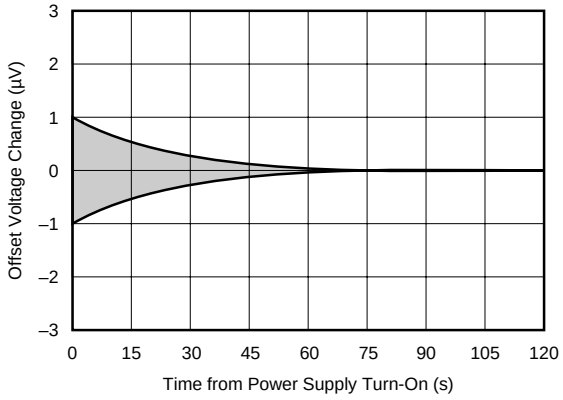

MAXIMUM $V_{OUT}$ vs $I_{OUT}$ (Negative Swing)



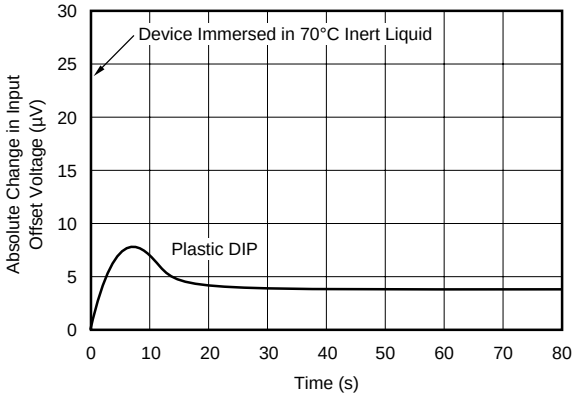

MAXIMUM $V_{OUT}$ vs $I_{OUT}$ (Positive Swing)



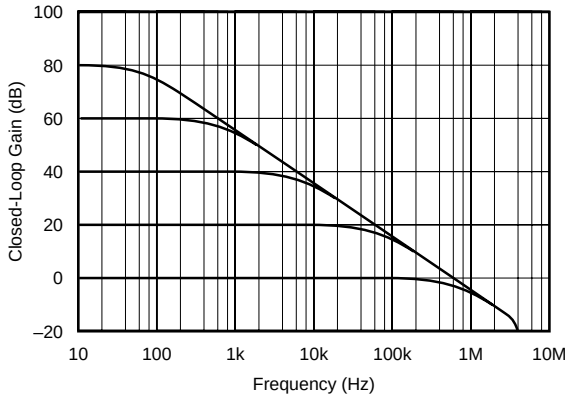

WARM-UP OFFSET VOLTAGE DRIFT




OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



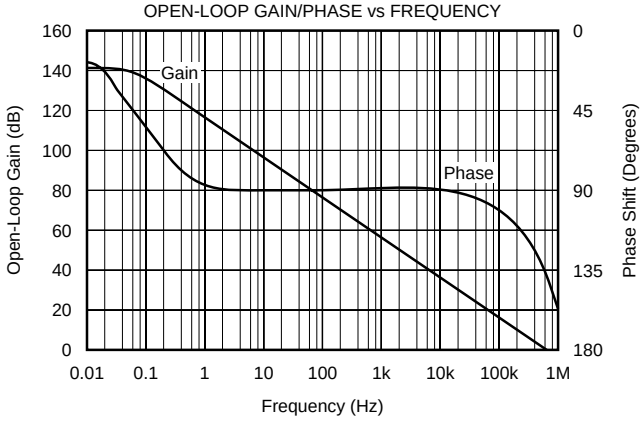

CLOSED-LOOP RESPONSE vs FREQUENCY



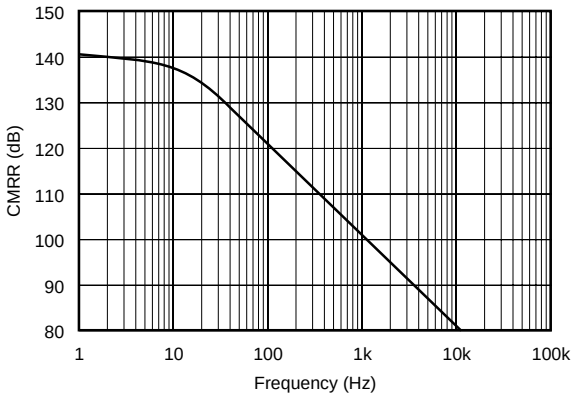
# TYPICAL PERFORMANCE CURVES (CONT)

At $T_A$ = +25°C, $V_S$ = ±15V, unless otherwise noted.

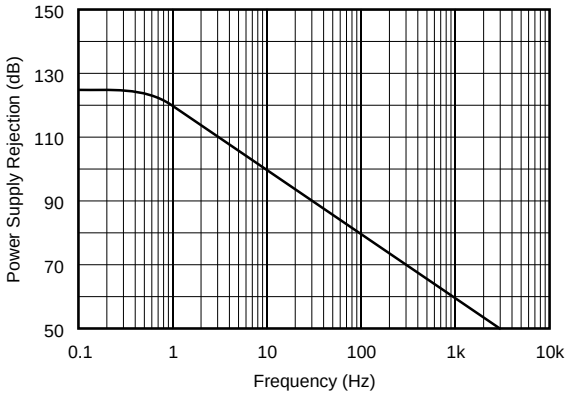
OPEN-LOOP GAIN/PHASE vs FREQUENCY



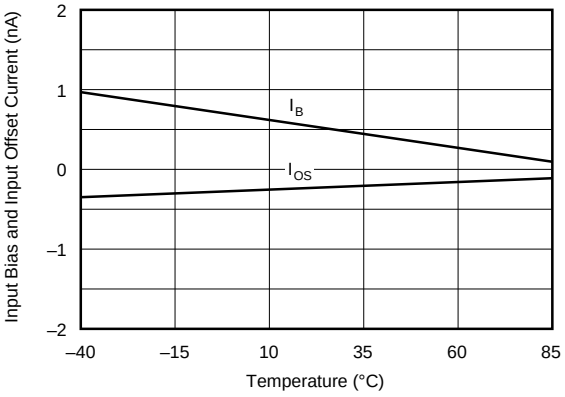

CMRR vs FREQUENCY



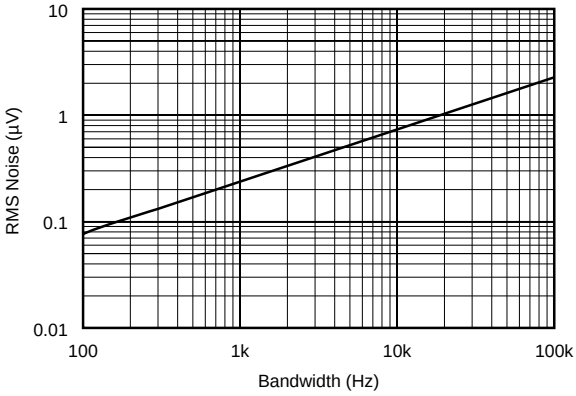

POWER SUPPLY REJECTION vs FREQUENCY



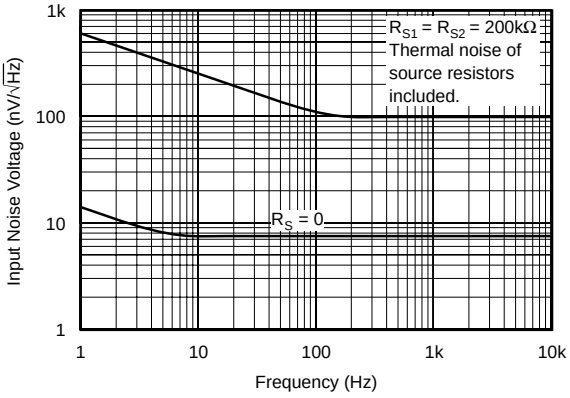

INPUT BIAS AND INPUT OFFSET CURRENT vs TEMPERATURE




TOTAL NOISE vs BANDWIDTH (0.1Hz to Frequency Indicated)



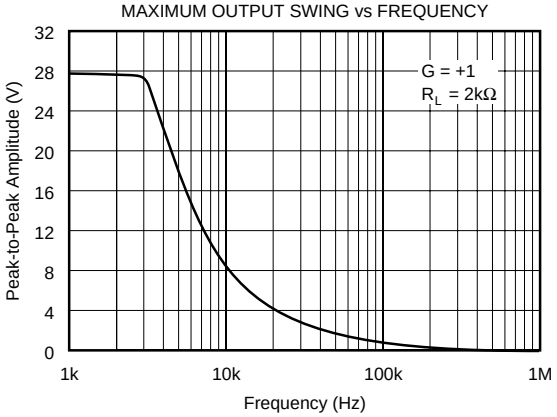

INPUT NOISE VOLTAGE DENSITY vs FREQUENCY



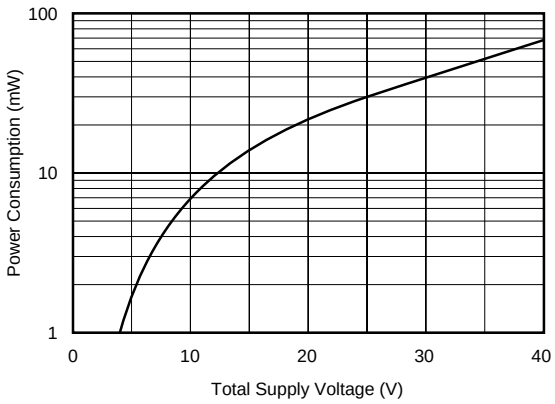
# TYPICAL PERFORMANCE CURVES (CONT)

At $T_A$ = +25°C, $V_S$ = ±15V, unless otherwise noted.

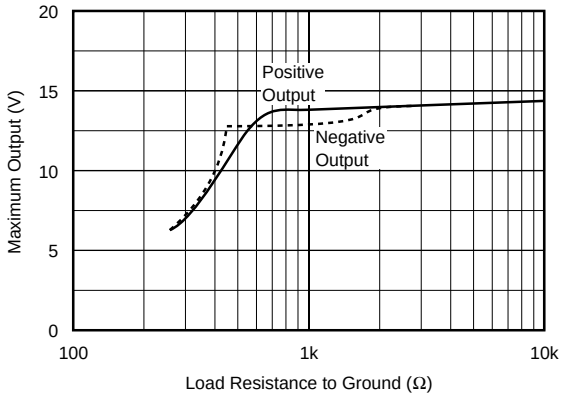
MAXIMUM OUTPUT SWING vs FREQUENCY



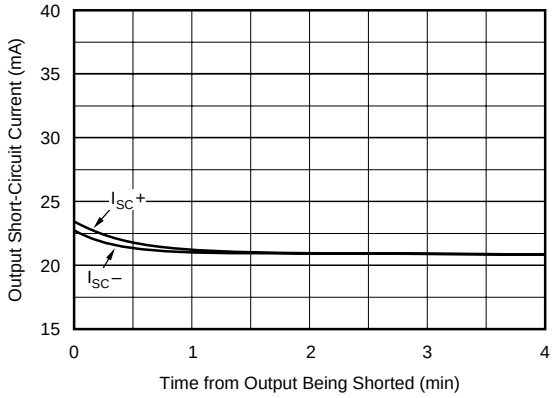

POWER CONSUMPTION vs POWER SUPPLY




MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE




OUTPUT SHORT-CIRCUIT CURRENT vs TIME



# APPLICATIONS INFORMATION

The OPA177 is unity-gain stable, making it easy to use and free from oscillations in the widest range of circuitry. Applications with noisy or high impedance power supply lines may require decoupling capacitors close to the device pins. In most cases 0.1µF ceramic capacitors are adequate.

The OPA177 has very low offset voltage and drift. To achieve highest performance, circuit layout and mechanical conditions must be optimized. Offset voltage and drift can be degraded by small thermoelectric potentials at the op amp inputs. Connections of dissimilar metals will generate thermal potential which can mask the ultimate performance of the OPA177. These thermal potentials can be made to cancel by assuring that they are equal in both input terminals.

1. Keep connections made to the two input terminals close together.
2. Locate heat sources as far as possible from the critical input circuitry.
3. Shield the op amp and input circuitry from air currents such as cooling fans.

## OFFSET VOLTAGE ADJUSTMENT

The OPA177 has been laser-trimmed for low offset voltage and drift so most circuits will not require external adjustment. Figure 1 shows the optional connection of an external potentiometer to adjust offset voltage. This adjustment should not be used to compensate for offsets created elsewhere in a system since this can introduce excessive temperature drift.

## INPUT PROTECTION

The inputs of the OPA177 are protected with 500Ω series input resistors and diode clamps as shown in the simplified circuit diagram. The inputs can withstand ±30V differential inputs without damage. The protection diodes will, of course, conduct current when the inputs are overdriven. This may disturb the slewing behavior of unity-gain follower applications, but will not damage the op amp.

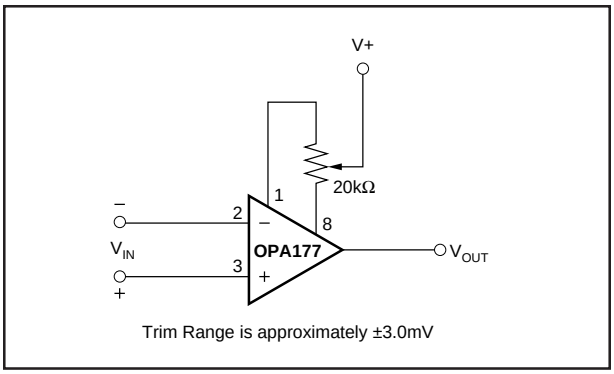



FIGURE 1. Optional Offset Nulling Circuit.

## NOISE PERFORMANCE

The noise performance of the OPA177 is optimized for circuit impedances in the range of 2kΩ to 50kΩ. Total noise in an application is a combination of the op amp's input voltage noise and input bias current noise reacting with circuit impedances. For applications with higher source impedance, the OPA627 FET-input op amp will generally provide lower noise. For very low impedance applications, the OPA27 will provide lower noise.

## INPUT BIAS CURRENT CANCELLATION

The input stage base current of the OPA177 is internally compensated with an equal and opposite cancellation current. The resulting input bias current is the difference between the input stage base current and the cancellation current. This residual input bias current can be positive or negative.

When the bias current is cancelled in this manner, the input bias current and input offset current are approximately the same magnitude. As a result, it is not necessary to balance the DC resistance seen at the two input terminals (Figure 2). A resistor added to balance the input resistances may actually increase offset and noise.

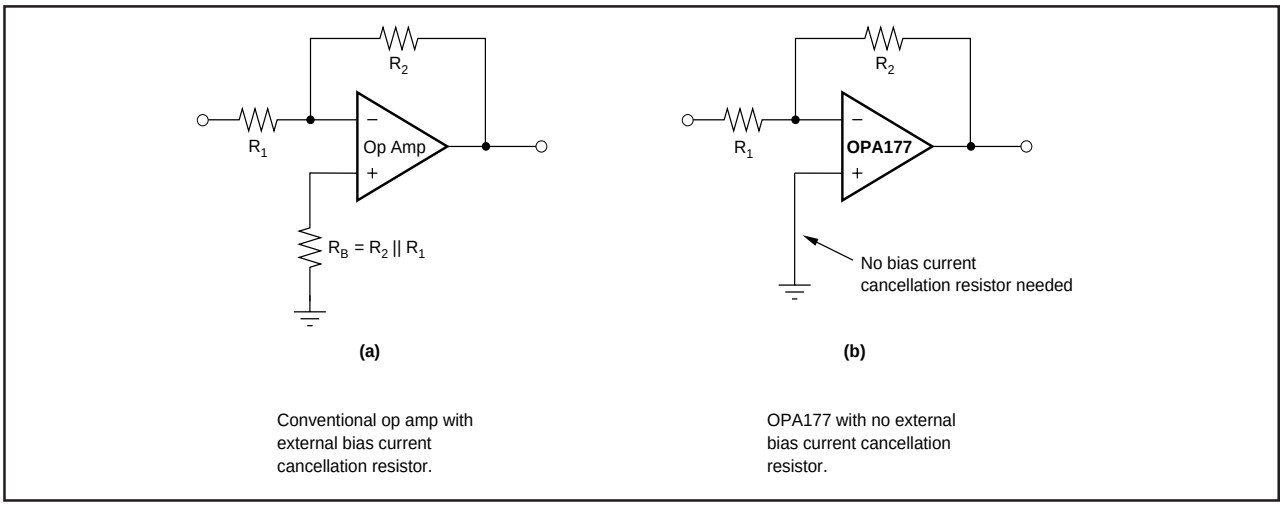



FIGURE 2. Input Bias Current Cancellation.

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| OPA177FP | ACTIVE | PDIP | P | 8 | 50 | None | Call TI | Level-NA-NA-NA |
| OPA177GP | ACTIVE | PDIP | P | 8 | 50 | None | Call TI | Level-NA-NA-NA |
| OPA177GS | ACTIVE | SOIC | D | 8 | 100 | None | CU SNPB | Level-3-220C-168 HR |
| OPA177GS/2K5 | ACTIVE | SOIC | D | 8 | 2500 | None | CU SNPB | Level-3-220C-168 HR |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**None:** Not yet available Lead (Pb-Free).
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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